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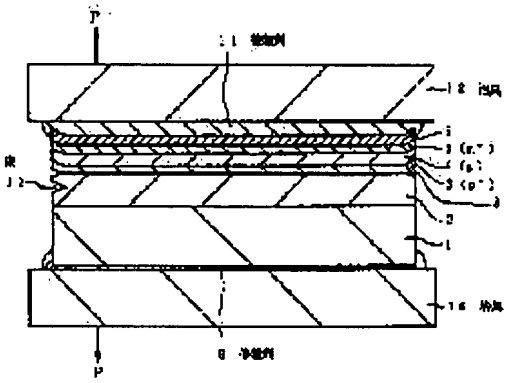
(54) METHOD OF SEPARATING ELEMENT FORMATION LAYER FROM BASE BODY

(57)Abstract:

PURPOSE: To provide a method of separating an element formation layer from a base body, which can manufacture a high-performance thin film element, such as a high-conversion efficiency thin film solar cell, at low cost.



CONSTITUTION: A porous Si later 2 is formed on a single crystal Si substrata 1 and a p+ Si layer 3, a p-type Si layer 4 and an n+ Si layer 5, which are used as a solar cell layer, are formed on the layer 2. After a protective film 6 is formed on the layer 5, the rear of the substrate 1 is bonded to a jig 10 and at the same time, a jig 12 is bonded to the surface of the film 6. Then, the layer 2 is mechanically broken by pulling the jigs 10 and 12 in the opposite direction to each other and the solar cell layer is separated from the substrate 1. This solar cell layer is held between two sheets of plastic substrates to manufacture a flexible thin film solar cell.

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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] How to separate the component formative layer from the base characterized by making it separate the above-mentioned component formative layer from the above-mentioned base by forming the component formative layer through a detached core on a base, and making fracture cause mechanically by the interface with the interior of the account detached core of Gokami and/or the above-mentioned detached core, the above-mentioned component formative layer, and the above-mentioned base.
[Claim 2] The mechanical strength of the above-mentioned detached core is the approach of separating the component formative layer from the base according to claim 1 characterized by being weaker than the mechanical strength of the above-mentioned base and the above-mentioned component formative layer.
[Claim 3] The above-mentioned detached core is the approach of separating the component formative layer from the base according to claim 1 characterized by being porosity.
[Claim 4] The above-mentioned detached core is the approach of separating the component formative layer from the base according to claim 1 characterized by being polycrystal.
[Claim 5] The above-mentioned detached core is the approach of separating the component formative layer from the base according to claim 1 characterized by the amorphous thing.
[Claim 6] The above-mentioned detached core is the approach of separating the component formative layer from the base according to claim 1 characterized by consisting of a semi-conductor.
[Claim 7] The above-mentioned detached core is the approach of separating the component formative layer from the base according to claim 1 characterized by consisting of silicon.
[Claim 8] The above-mentioned base is the approach of separating the component formative layer from the base according to claim 1 characterized by being a single crystal.
[Claim 9] The above-mentioned base is the approach of separating the component formative layer from the base according to claim 1 characterized by being polycrystal.
[Claim 10] The above-mentioned base is the approach of separating the component formative layer from the base according to claim 1 characterized by consisting of single crystal silicon.
[Claim 11] The above-mentioned base is the approach of separating the component formative layer from the base according to claim 1 characterized by consisting of cast polycrystalline silicon.
[Claim 12] The above-mentioned component formative layer is the approach of separating the component formative layer from the base according to claim 1 characterized by consisting of a semi-conductor.
[Claim 13] The above-mentioned component formative layer is the approach of separating the component formative layer from the base according to claim 1 characterized by consisting of single crystal silicon.
[Claim 14] How to separate the component formative layer from the base according to claim 1 characterized by making it make fracture cause mechanically by the interface with the interior of the above-mentioned detached core and/or the above-mentioned detached core, the above-mentioned

component formative layer, and the above-mentioned base by pulling the above-mentioned base and the above-mentioned component formative layer of each other to an opposite direction.
[Claim 15] While pasting up the above-mentioned detached core of the above-mentioned base, and the principal plane of the opposite side on the 1st fixture The above-mentioned detached core of the above-mentioned component formative layer and the principal plane of the opposite side are pasted up on the 2nd fixture. By pulling the 1st fixture of the above, and the 2nd fixture of each other of the above to an opposite direction How to separate the component formative layer from the base according to claim 1 characterized by making it make fracture cause mechanically by the interface with the interior of the above-mentioned detached core and/or the above-mentioned detached core, the above-mentioned component formative layer, and the above-mentioned base.
[Claim 16] How to separate the component formative layer from the base according to claim 1 characterized by forming the above-mentioned detached core which consists of porosity silicon by carrying out anodization of the above-mentioned base which consists of single crystal silicon, and forming the above-mentioned component formative layer which consists of single crystal silicon on the above-mentioned detached core.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention applies to manufacture of a thin film solar cell, concerning the approach of separating the component formative layer from a base, and is suitable.
[0002]
[Description of the Prior Art] After the solar battery was invented, about 40 years have passed. Although a part of solar battery is put in practical use, especially in order to be used completely, low-cost-izing is important. Moreover, in the semantics of preventing warming of earth environment, energy-recovery years need to become one or less year. Therefore, in order to reduce the energy which manufacture of a solar battery takes as much as possible, the thin film solar cell will be more desirable than the thick-film solar battery which manufacture takes much energy.
[0003] On the other hand, since a thin film solar cell can be bent to some extent, it can be generated by carrying in the curved-surface section of the curved-surface section of the body of an automobile, or the exterior of a portable electrical-and-electric-equipment product. Or it also becomes possible to fold up, when this thin film solar cell is applied to a solar battery charger, and extending when using a thin film solar cell, and not using it.
[0004] Conventionally, there is an amorphous-silicon solar cell formed on the plastic plate as such a thin film solar cell. However, while using this amorphous-silicon solar cell for the top where the conversion efficiency of photo electric conversion is low, it has the problem that conversion efficiency falls. For this reason, compared with the amorphous silicon, implementation of the thin film solar cell using single crystal silicon or polycrystalline silicon with high conversion efficiency was desired.
[0005]
[Problem(s) to be Solved by the Invention] However, since the process temperature which forms single crystal silicon or polycrystalline silicon was quite high, it was difficult to form on a plastic plate or a glass substrate.
[0006] This invention solves the above-mentioned problem which the conventional technique has.
[0007] That is, the purpose of this invention is to offer the approach of separating the component formative layer from the base which can manufacture the thin film of high performance, such as a thin film solar cell of high conversion efficiency, by low cost.
[0008]
[Means for Solving the Problem] In order to attain the above-mentioned purpose, the method of separating the component formative layer from the base by this invention forms the component formative layer through a detached core on a base, and is characterized by making it separate the component formative layer from a base by making fracture cause mechanically after that by the interface with the interior of a detached core and/or a detached core, the component formative layer, and a base.
[0009] Typically in this invention, the mechanical strength of a detached core is weaker than the mechanical strength of a base and the component formative layer.
[0010] In this invention, a detached core is porosity, polycrystal, or an amorphous substance.

[0011] Typically in this invention, a detached core consists of a semi-conductor. This semi-conductor may be an elemental semiconductor, or may be a compound semiconductor. A former example is silicon (Si) and a latter example is gallium arsenide (GaAs).
[0012] In this invention, suitably, although a base is a single crystal, polycrystal is sufficient.
[0013] In this invention, suitably, although a base consists of single crystal silicon, it may consist of cast polycrystalline silicon, for example.
[0014] Typically in this invention, the component formative layer consists of a semi-conductor. In this case, a component is a semiconductor device.
[0015] The component formative layer consists of single crystal silicon in 1 suitable operation gestalt of this invention.
[0016] Fracture is made to cause mechanically typically in this invention by the interface with the interior of a detached core and/or a detached core, the component formative layer, and a base by pulling a base and the component formative layer of each other to an opposite direction. While pasting up the detached core of a base, and the principal plane of the opposite side on the 1st fixture, the detached core of the component formative layer and the principal plane of the opposite side are pasted up on the 2nd fixture, and fracture is made to cause mechanically in practice by the interface with the interior of a detached core and/or a detached core, the component formative layer, and a base by pulling the 1st fixture and 2nd fixture of each other to an opposite direction.
[0017] In 1 typical operation gestalt of this invention, by carrying out anodization of the base which consists of single crystal silicon, the detached core which consists of porosity silicon is formed, and the component formative layer which consists of single crystal silicon is formed on a detached core.
[0018] In this invention, after performing mechanical fracture of a detached core typically, polish and/or etching remove the detached core left behind on the base, and it removes similarly the detached core left behind to the rear face of the component formative layer by polish and/or etching. Thus, the separated base is used again. What is necessary is to grow up the same matter as this base on a base, and just to make it restore to the original thickness here, in order to compensate reduction of that thickness, in forming a detached core using the process in which the thickness of bases, such as anodization, decreases.
[0019] In this invention, when the component formative layer may be used for various kinds of components and that example is given, it is a solar-battery layer in a thin film solar cell.
[0020]
[Function] Since he is trying to separate the component formative layer from a base by making fracture cause mechanically by the interface with the interior of a detached core and/or a detached core, the component formative layer, and a base according to this invention constituted as mentioned above, a thin film, for example, a thin film solar cell, can be manufactured by forming this component formative layer in the thin film using the component formative layer of this thin film. In this case, a thin film, for example, a thin film solar cell, can be manufactured by low cost that the component formative layer is a thin film, by the ability repeating and using a base, since polish, etching, etc. of a base are not performed in order to separate the component formative layer, etc. Furthermore, by forming the component formative layer in a single crystal or polycrystal, if it is in the thin film of high performance, especially a thin film solar cell, the thing of high conversion efficiency can be obtained. Moreover, since this thin film, for example, a thin film solar cell, can be bent to some extent, a flexible thin film, for example, a flexible thin film solar cell, can be obtained.
[0021]
[Example] Hereafter, it explains, referring to a drawing about the example of this invention. In addition, in the complete diagram of an example, the sign identically same into a corresponding part is attached.
[0022] Drawing 1 - drawing 10 are the sectional views showing the manufacture approach of the thin film solar cell by the 1st example of this invention in order of a process.
[0023] In the manufacture approach of the thin film solar cell by this 1st example, first, as shown in drawing 1 , the porosity Si layer 2 is formed by carrying out anodization (anodic oxidation) of the single crystal Si substrate 1. When the formation approach of the porosity Si layer 2 by this anodization

method is learned well (for example, the 57th volume of application physics, No. 11, the 1710th page (1988)), for example, current density is set to 30mA and HF:H2 O:C2 H5 OH=1:1:1 are used as an anodization solution, the thickness of the porosity Si layer 2 obtained is 5-50 micrometers, and porosity (porosity) is 10 - 50%. In order to lessen reduction of the thickness of this single crystal Si substrate 1 and to make [many] the count of usable, as for the thickness of this porosity Si layer 2, it is desirable to make it as thin as possible, and it is suitably chosen as 5-15 micrometers, for example, about 10 micrometers, from a viewpoint which repeats and uses the single crystal Si substrate 1. Moreover, although it is desirable that it is p mold from a viewpoint which forms the porosity Si layer 2 on it by anodization as for the single crystal Si substrate 1, even if it is n mold, it is possible to form the porosity Si layer 2 depending on conditioning.

[0024] Next, as shown in drawing 2 , it is p+ at the temperature of 700-1100 degrees C by the CVD method on the porosity Si layer 2. The mold Si layer 3, the p mold Si layer 4, and n+ n+ after carrying out sequential epitaxial growth of the mold Si layer 5 It is SiO2 of a monolayer by the CVD method on the mold Si layer 5. The protective coat 6 which consists of the film, SiN films, or those cascade screens is formed. Here, it is p+. The mold Si layer 3, the p mold Si layer 4, and n+ The mold Si layer 5 constitutes a solar-battery layer, and the thickness of those sum totals is 1-50 micrometers, for example, 5 micrometers, typically. Moreover, these p+ that constitutes a solar-battery layer in this case The mold Si layer 3, the p mold Si layer 4, and n+ In order to make the crystallinity of the mold Si layer 5 good, While forming an oxide film thin to the wall of the hole of the interior before those epitaxial growth by carrying out short-time oxidation of the porosity Si layer 2 at the temperature of 400-600 degrees C and raising the reinforcement For example, it sets in a vacuum, for example, is H2 at the temperature of 950-1000 degrees C. By annealing, the hole of the front face of the porosity Si layer 2 is buried as much as possible, and it is desirable that epitaxial growth is made to be performed good. By doing in this way, it is p+ of a single crystal. The mold Si layer 3, the p mold Si layer 4, and n+ The mold Si layer 5 can be obtained (for example, a Nikkei micro device, the July, 1994 issue, the 76th page).

[0025] Next, as shown in drawing 3 , they are the porosity Si layer 2 and p+ as mentioned above. The mold Si layer 3, the p mold Si layer 4, and n+ SiO2 whose thickness is 50-500nm on the whole front face by oxidizing thermally the whole single crystal Si substrate 1 with which the mold Si layer 5 and the protective coat 6 were formed The oxide film 7 which consists of film is formed. Since the oxidation rate of the porosity Si layer 2 is quicker than the oxidation rate of the single crystal Si substrate 1 at the time of this thermal oxidation and the volume of the porosity Si layer 2 expands at it, The porosity Si layer 2 and p+ in the edge section p+ [in / an oxide film 7 is formed in an interface with the mold Si layer 3 in the shape of a BAZU beak, and / the edge section] The mold Si layer 3, the p mold Si layer 4, and n+ It becomes the structure in which the mold Si layer 5 and the whole protective coat 6 were raised.

[0026] Next, etching removal of the oxide film 7 is carried out. The porosity Si layer 2 and p+ The wedge-shaped gap 8 is formed between the mold Si layers 3. [in / as this shows to drawing 4 / the edge section] This wedge-shaped gap 8 is for performing easily fracture by hauling of the porosity Si layer 2 at a next process.

[0027] Next, as shown in drawing 5 , while pasting up the rear face of the single crystal Si substrate 1 on a fixture 10 with adhesives 9, another fixture 12 is pasted up on the front face of a protective coat 6 with adhesives 11. What what has sufficient reinforcement to which these fixtures 10 and 12 can bear hauling performed at a next process is used, for example, consists of a metal, a quartz, etc. is used. Moreover, what has sufficient bond strength to which adhesives 9 and 11 can bear hauling performed at a next process is used, for example, an instantaneous adhesive etc. is used. Furthermore, in order to enable it to perform more easily fracture by hauling of the porosity Si layer 2 at a next process in this case, the blemish 13 is beforehand attached to the side attachment wall of the edge section of the porosity Si layer 2. This blemish 13 can be attached by the mechanical approach, and also it can also be attached by the exposure of a laser beam etc.

[0028] Next, as shown in drawing 5 , the external force P big enough is applied and pulled to fixtures 10 and 12. It is made for stress concentration to occur in the edge section of the porosity Si layer 2 at this

time in addition to the location where this external force P shifted from the core of the single crystal Si substrate 1 to the edge section side in which it has the blemish 13 of the porosity Si layer 2. Consequently, it adds to the porosity Si layer 2 having a low mechanical strength in itself. The porosity Si layer 2 and p+ in pre-having the blemish 13 on the side attachment wall of the edge section of the porosity Si layer 2, or the edge section Stress concentration breaks out very notably in these locations by forming the wedge-shaped gap 8 between the mold Si layers 3. As shown in drawing 6 , they are the interior of the porosity Si layer 2, the porosity Si layer 2, and p+. Fracture breaks out by the interface with the mold Si layer 3. By this, it is [the single crystal Si substrate 1 and] p+. The mold Si layer 3, the p mold Si layer 4, and n+ The mold Si layer 5 and the protective coat 6 of each other are separated.

[0029] Next, it is the porosity Si layer 2 left behind to the front face of the single crystal Si substrate 1, and the front face of the p+ mold Si layer 3 after above-mentioned fracture, respectively as shown in drawing 7 HF/H 2O2 Etching removal is carried out using an etching reagent [like]. After removing adhesives 9 and removing a fixture 10, the single crystal Si substrate 1 grinds the front face, and is again used as a substrate for thin film solar cell manufacture. Here, supposing the thickness removed by the polish for carrying out the reuse of 10 micrometers and the single crystal Si substrate 1 for the thickness of the porosity Si layer 2 is about 3 micrometers, the thickness of the single crystal Si substrate 1 which decrease in number in 1 cycle of manufacture of a thin film solar cell is 13 micrometers. Therefore, since reduction of the thickness of the single crystal Si substrate 1 is only 130 micrometers even if it uses the single crystal Si substrate 1 10 times, it is usually possible to use the single crystal Si substrate 1 at least 10 times.

[0030] Next, it is p+ as shown in drawing 8 . The front face which the mold Si layer 3 exposed is pasted up on the front face of a glass substrate 14 with adhesives 15. As these adhesives 15, the thing of for example, an epoxy resin system is used.

[0031] Next, after removing adhesives 11 and removing a fixture 12 from a protective coat 6, as it is shown in drawing 9 , etching removal of the predetermined part of a protective coat 6 is carried out, opening 6a is formed, this opening 6a is led, and it is n+. The light-receiving side electrode 16 is formed on the mold Si layer 5. This light-receiving side electrode 16 is formed by print processes. Then, the metal layer 16 of the same configuration as this light-receiving side electrode 16 prepares the plastic plate 18 formed beforehand, and connects these light-receiving side electrodes 16 and metal layer 17 comrades to the part corresponding to this light-receiving side electrode 16. Since a clearance is formed between a protective coat 6 and a plastic plate 18 at this time, this clearance is filled up with the transparent adhesives 19 of an epoxy resin system, and a protective coat 6 and a plastic plate 18 are pasted up.

[0032] Next, adhesives 15 are removed and it is p+. After removing a glass substrate 14 from the mold Si layer 3, as it is shown in drawing 10 , it is p+ by print processes. The rear-face electrode 20 is formed on the mold Si layer 3, and a plastic plate 22 is pasted up on this rear-face electrode 20 with adhesives 21. Here, this rear-face electrode 20 also serves as a reflecting plate of the incident light to a thin film solar cell, and is contributed to high conversion efficiency-ization.

[0033] p+ which constitutes a solar-battery layer by the above The thin film solar cell which the mold Si layer 3, the p mold Si layer 4 and the n+ mold Si layer 5, and a protective coat 6 make the purpose of the structure where it was inserted between the plastic plate 18 of two sheets and 22 is completed.

[0034] As mentioned above, p+ of the single crystal which constitutes a solar-battery layer through the porosity Si layer 2 on the single crystal Si substrate 1 according to this 1st example The mold Si layer 3, the p mold Si layer 4, and n+ After carrying out sequential epitaxial growth of the mold Si layer 5, The porosity Si layer 2 is mechanically fractured by hauling, this solar-battery layer is separated from the single crystal Si substrate 1, and the thin film solar cell is manufactured by pinching this solar-battery layer between the plastic plate 18 of two sheets, and 22. In this case, when a solar-battery layer is a single crystal, this thin film solar cell is high conversion efficiency, and is excellent also in dependability. Moreover, this thin film solar cell can be manufactured by low cost that the single crystal Si substrate 1 can be repeated and used, using the mechanical approach for separation of the solar-battery layer from the single crystal Si substrate 1, by using the cheap plastic plates 18 and 22, etc.

Moreover, a solar-battery layer is thin, by using that it can bend to some extent in itself and the flexible plastic plates 18 and 22 etc., this thin film solar cell can be carried, for example in the curved-surface section of the curved-surface section of the body of an automobile, or the exterior of a portable electrical-and-electric-equipment product from bending being possible to some extent as a whole, and its application range is wide.

[0035] That is, according to this 1st example, a thin film solar cell with flexible high conversion efficiency and high-reliability can be manufactured by low cost.

[0036] Next, the 2nd example of this invention is explained.

[0037] In the manufacture approach of the thin film solar cell by the 1st above-mentioned example They are the single crystal Si substrate 1 and p+ by fracture of the porosity Si layer 2. The mold Si layer 3, the p mold Si layer 4, and n+ As opposed to having applied external force P to fixtures 10 and 12, as shown in drawing 5 when separating the mold Si layer 5 and an insulator layer 6 By applying external force P to fixtures 10 and 12, as the manufacture approach of the thin film solar cell by this 2nd example is shown in drawing 11 , the porosity Si layer 2 is fractured and they are the single crystal Si substrate 1 and p+. The mold Si layer 3, the p mold Si layer 4, and n+ The mold Si layer 5 and an insulator layer 6 are separated. Since the thing of others of the manufacture approach of the thin film solar cell by this 2nd example is the same as that of the manufacture approach of the thin film solar cell by the 1st example, explanation is omitted.

[0038] According to this 2nd example as well as the 1st example, a thin film solar cell with flexible high conversion efficiency and high-reliability can be manufactured by low cost.

[0039] Next, the 3rd example of this invention is explained.

[0040] It is p+ as the manufacture approach of the thin film solar cell by the 1st above-mentioned example is shown in drawing 10 . Since the whole surface of the mold Si layer 3 touches the rear-face electrode 20, it is this p+. The recombination of an electronic-electron hole pair generated by optical incidence in the interface of the mold Si layer 3 and the rear-face electrode 20 tends to break out, and there is a possibility that it may reduce conversion efficiency. Then, it sets to the manufacture approach of the thin film solar cell by this 3rd example. As shown in drawing 12 , it is SiO2 of a monolayer on the p+ mold Si layer 3. The protective coat 23 which consists of the film, SiN films, or those cascade screens is formed. Opening 23a is formed in this insulator layer 23, the rear-face electrode 24 is formed by print processes through this opening 23a, and this rear-face electrode 24 is connected with the metal layer 25 beforehand formed on the plastic plate 22. Since a clearance is formed between a protective coat 23 and the metal layer 25 at this time, this clearance is filled up with the transparent adhesives 26 of an epoxy resin system, and a protective coat 23 and the metal layer 25 are pasted up. Since the thing of others of the manufacture approach of the thin film solar cell by this 3rd example is the same as that of the manufacture approach of the thin film solar cell by the 1st example, explanation is omitted.

[0041] According to this 3rd example, it is p+. By the ability decreasing sharply the recombination of an electronic-electron hole pair in the interface of the mold Si layer 3 and the rear-face electrode 24, conversion efficiency of a thin film solar cell can be made higher compared with the 1st example, and also there is the same advantage as the 1st example.

[0042] Next, the 4th example of this invention is explained.

[0043] In the manufacture approach of the thin film solar cell by the 1st above-mentioned example Although he is trying to paste up this solar-battery layer on a plastic plate 22 in the process shown in drawing 10 after once pasting up the rear face of a solar-battery layer on a glass substrate 14 in the process shown in drawing 8 and removing this glass substrate 14 after that In the manufacture approach of the thin film solar cell by this 4th example, a solar-battery layer is not pasted up on a glass substrate 14, but it is p+. The direct rear-face electrode 20 is formed in the mold Si layer 3 by print processes, and this rear-face electrode 20 is pasted up on a plastic plate 22 with adhesives 21. Then, while removing adhesives 11, removing a fixture 12 and forming opening 6a in a protective coat 6, the light-receiving side electrode 16 is formed and this light-receiving side electrode 16 and the metal layer 17 on a plastic plate 18 are connected, and the clearance between a protective coat 6 and a plastic plate 18 is further filled up with adhesives 19, and it pastes up. Since the thing of others of the manufacture approach of

the thin film solar cell by this 4th example is the same as that of the manufacture approach of the thin film solar cell by the 1st example, explanation is omitted.
[0044] According to this 4th example, simplification of a production process can be attained compared with the 1st example, therefore there is an advantage that a thin film solar cell can be manufactured more by low cost.
[0045] Next, the 5th example of this invention is explained.
[0046] In the manufacture approach of the thin film solar cell by the 1st above-mentioned example, although the light-receiving side electrode 16 was formed in the process shown in drawing 9 , while forming opening 6a in a protective coat 6 in the process shown in drawing 3 , the light-receiving side electrode 16 is formed in the manufacture approach of the thin film solar cell by this 5th example. Since the thing of others of the manufacture approach of the thin film solar cell by this 5th example is the same as that of the manufacture approach of the thin film solar cell by the 1st example, explanation is omitted.

[0047] Also according to this 5th example, the same advantage as the 1st example can be acquired.
[0048] Next, the 6th example of this invention is explained.
[0049] A solar-battery layer is made into double hetero structure in the manufacture approach of the thin film solar cell by this 6th example. That is, as this 6th example is shown in drawing 13 , it is p+ on the porosity Si layer 2. The mold Si layer 31 and p mold Si1-x Gex Graded layer 32, for example, Si1-y Gey of undoping, A layer 33 and n mold Si1-x Gex A graded layer 34 and n+ Sequential epitaxial growth of the mold Si layer 35 is carried out, and the solar-battery layer of double hetero structure is formed. In this case, p mold Si1-x Gex germanium presentation ratio x of a graded layer 32 This p mold Si1-x Gex In the thickness direction of a graded layer 32 p+ The mold Si layer 31 and this p mold Si1-x Gex The value of 0 in an interface with a graded layer 32 to Si1-y Gey A layer 33 and this p mold Si1-x Gex It is increasing in monotone to the value of y in an interface with a graded layer 32. Moreover, n mold Si1-x Gex germanium presentation ratio x of a graded layer 34 This n mold Si1-x Gex In the thickness direction of a graded layer 34 n+ The mold Si layer 35 and this n mold Si1-xGex The value of 0 in an interface with a graded layer 34 to Si1-y Gey A layer 33 and this p mold Si1-x Gex It is increasing in monotone to the value of y in an interface with a graded layer 34. By this, they are these p+. The mold Si layer 31 and p mold Si1-x Gex A graded layer 32 and Si1-y Gey A layer 33 and n mold Si1-x Gex A graded layer 34 and n+ Good crystallinity can be acquired from a grid having consistency in the field side between the mold Si layers 35. Since the thing of others of the manufacture approach of the thin film solar cell by this 6th example is the same as that of the manufacture approach of the thin film solar cell by the 1st example, explanation is omitted.
[0050] According to this 6th example, a solar-battery layer is double hetero structure, and it is Si1-y Gey of that center. High conversion efficiency can be acquired by the ability confining a carrier and light in a layer 33 effectively, and also there are the same various advantages as the 1st example.
[0051] Next, the 7th example of this invention is explained. This 7th example is an example which applied this invention to manufacture of a CMOS mold semiconductor device.
[0052] In the manufacture approach of the CMOS mold semiconductor device by this 7th example, as shown in drawing 14 , after forming the porosity Si layer 2 on the single crystal Si substrate 1 first, epitaxial growth of the p mold Si layer 41 of a single crystal is carried out with a CVD method on this porosity Si layer 2. Although the thickness of this p mold Si layer 41 is chosen if needed, it is set to 5 micrometers, for example. Moreover, high impurity concentration of this p mold Si layer 41 is made about [1015cm -] into three.
[0053] Next, as shown in drawing 15 , into this p mold Si layer 41, n mold impurity is alternatively doped with ion-implantation or a thermal diffusion method, and n wells 42 are formed. Next, it is SiO2 for example, by the oxidizing [thermally] method on the p mold Si layer 41. After forming gate dielectric film 43 like the film, the gate electrodes 44 and 45 are formed on this gate dielectric film 43. Here, these gate electrodes 44 and 45 form the polycrystal Si film with a CVD method for example, on gate dielectric film 43, and after they dope and form an impurity into low resistance on this polycrystal Si film, they form it by carrying out patterning of the polycrystal Si film with which this impurity was

doped by etching.
[0054] Next, n+ used as a source field or a drain field by carrying out the ion implantation of the n mold impurity into the p mold Si layer 41 by using the gate electrode 44 as a mask where the front face of the part of n wells 42 is covered with a mask The mold fields 46 and 47 are formed in self align to the gate electrode 44. next, n after removing the mask used for the ion implantation of this n mold impurity -- the condition of having formed the mask according to wrap for the front face of the part except the part of a well 42 -- the gate electrode 45 -- a mask -- carrying out -- n -- p+ used as a source field or a drain field by carrying out the ion implantation of the p mold impurity into a well 42 The mold fields 48 and 49 are formed in self align to the gate electrode 45.
[0055] Next, it is SiO2 to the whole surface, for example by the CVD method. After forming an interlayer insulation film 50 like the film, etching removal of the predetermined part of this interlayer insulation film 50 is carried out, and contact holes 50a, 50b, 50c, and 50d are formed. Next, after forming for example, aluminum film in the whole surface, for example with the sputtering method or vacuum evaporation technique, patterning of this aluminum film is carried out by etching, and electrodes 51, 52, 53, and 54 are formed. In this case, the gate electrode 44 and n+ An n channel MOS transistor is formed of the mold fields 46 and 47, and they are the gate electrode 45 and p+. A p channel MOS transistor is formed of the mold fields 48 and 49. And CMOS is formed of these n channel MOS transistors and a p channel MOS transistor.
[0056] Next, similarly, if shown in drawing 5 of the 1st example, while pasting up the rear face of the single crystal Si substrate 1 on a fixture 10 with adhesives 9, a fixture 12 will be pasted up on the front face of a CMOS mold semiconductor device with adhesives 11. Next, by applying external force P to these fixtures 10 and 12, and pulling to an opposite direction mutually, the porosity Si layer 2 is fractured and a CMOS mold semiconductor device is separated from the single crystal Si substrate 1.
[0057] Next, after removing the remaining porosity Si layers 2 from the rear face of the p mold Si layer 41 and removing fixtures 10 and 12 further, as shown in drawing 16 , the rear face of this p mold Si layer 41 is stretched with the heat sink 55 which consists of a metal with a silver paste etc. Then, chip-ization (pelletizing) is performed if needed.
[0058] By the above, the CMOS mold semiconductor device which has a heat sink 55 is manufactured by the rear face of the p mold Si layer 41.
[0059] According to this 7th example, when the p mold Si layer 41 which constitutes a barrier layer is a single crystal, the CMOS mold semiconductor device which has the high engine performance which is equal to CMOS by bulk Si can be manufactured by low cost. Moreover, by forming the heat sink 55 in the rear face of the p mold Si layer 41 of this CMOS mold semiconductor device, the temperature rise at the time of actuation can be lessened, and the performance degradation and the defect accompanying a temperature rise can be prevented.
[0060] Next, the 8th example of this invention is explained. This 8th example is an example which applied this invention to manufacture of the semiconductor laser of double hetero structure.
[0061] In the manufacture approach of the semiconductor laser by this 8th example, as shown in drawing 17 , the porosity GaAs layer 62 is first formed on the single crystal GaAs substrate 61. Next, epitaxial growth of the n mold GaAs layer 63 is carried out on this porosity GaAs layer 62, on this n mold GaAs layer 63, sequential epitaxial growth of the n mold AlGaAs layer 64 as an n mold cladding layer, the barrier layer 65 which consists of GaAs, and the p mold AlGaAs layer 66 as a p mold cladding layer is carried out, and laser structure is formed. In addition, although the thickness of the n mold GaAs layer 63 is chosen if needed, it is set to 5 micrometers, for example.
[0062] Next, similarly, if shown in drawing 5 of the 1st example, while pasting up the rear face of the single crystal GaAs substrate 61 on a fixture 10 with adhesives 9, a fixture 12 will be pasted up on the front face of the p mold AlGaAs layer 66 with adhesives 11. Next, by applying external force P to these fixtures 10 and 12, and pulling to an opposite direction mutually, the porosity GaAs layer 62 is fractured and the n mold GaAs layer 63, the n mold AlGaAs layer 64, a barrier layer 65, and the p mold AlGaAs layer 66 are separated from the single crystal GaAs substrate 61.
[0063] Next, after removing the porosity GaAs layer 62 left behind to the rear face of the n mold GaAs

layer 63 and removing fixtures 10 and 12 further, illustration is omitted, but while forming n lateral electrode in the rear face of this n mold GaAs layer 63, p lateral electrode is formed on the p mold AlGaAs layer 66, and the semiconductor laser of the double hetero structure made into the purpose is manufactured.

[0064] According to this 8th example, the semiconductor laser of double hetero structure can be manufactured by low cost. Moreover, in this semiconductor laser, although the n mold GaAs layer 63 plays the role of a substrate, since this n mold GaAs layer 63 is very thin compared with the n mold GaAs substrate usually used in semiconductor laser, series resistance by the substrate can be made very small, and only that part can aim at reduction of the operating voltage of semiconductor laser.

[0065] As mentioned above, although the example of this invention was explained concretely, this invention is not limited to an above-mentioned example, and various kinds of deformation based on the technical thought of this invention is possible for it.

[0066] For example, it sets in the 1st above-mentioned example, and is p+ by the CVD method on the porosity Si layer 2. The mold Si layer 3, the p mold Si layer 4, and n+ Although epitaxial growth of the mold Si layer 5 is carried out An amorphous Si layer is formed by a plasma-CVD method etc. on the porosity Si layer 2, and solid phase growth is carried out and you may make it crystallize this amorphous Si layer by performing annealing after that, for example, the temperature of 600-800 degrees C. In this case, when the porosity Si layer 2 serves as seed crystal, formation of a quality solid phase epitaxial layer is possible.

[0067] Moreover, Si1-y Gey in the 6th above-mentioned example germanium layer may be used instead of a layer 33.

[0068] Furthermore, this invention can also be applied to manufacture of for example, a SOI (silicon on insulator) substrate.

[0069]

[Effect of the Invention] Since he is trying to separate the component formative layer from a base by making fracture cause mechanically by the interface with the interior of a detached core and/or a detached core, the component formative layer, and a base according to this invention as explained above, the thin film of high performance, such as a thin film solar cell of high conversion efficiency, can be manufactured by low cost, for example.

[Translation done.]

* NOTICES *

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3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is a sectional view for explaining the manufacture approach of the thin film solar cell by the 1st example of this invention.
[Drawing 2] It is a sectional view for explaining the manufacture approach of the thin film solar cell by the 1st example of this invention.
[Drawing 3] It is a sectional view for explaining the manufacture approach of the thin film solar cell by the 1st example of this invention.
[Drawing 4] It is a sectional view for explaining the manufacture approach of the thin film solar cell by the 1st example of this invention.
[Drawing 5] It is a sectional view for explaining the manufacture approach of the thin film solar cell by the 1st example of this invention.
[Drawing 6] It is a sectional view for explaining the manufacture approach of the thin film solar cell by the 1st example of this invention.
[Drawing 7] It is a sectional view for explaining the manufacture approach of the thin film solar cell by the 1st example of this invention.
[Drawing 8] It is a sectional view for explaining the manufacture approach of the thin film solar cell by the 1st example of this invention.
[Drawing 9] It is a sectional view for explaining the manufacture approach of the thin film solar cell by the 1st example of this invention.
[Drawing 10] It is a sectional view for explaining the manufacture approach of the thin film solar cell by the 1st example of this invention.
[Drawing 11] It is a sectional view for explaining the manufacture approach of the thin film solar cell by the 2nd example of this invention.
[Drawing 12] It is a sectional view for explaining the manufacture approach of the thin film solar cell by the 3rd example of this invention.
[Drawing 13] It is a sectional view for explaining the manufacture approach of the thin film solar cell by the 6th example of this invention.
[Drawing 14] It is a sectional view for explaining the manufacture approach of the CMOS mold semiconductor device by the 7th example of this invention.
[Drawing 15] It is a sectional view for explaining the manufacture approach of the CMOS mold semiconductor device by the 7th example of this invention.
[Drawing 16] It is a sectional view for explaining the manufacture approach of the CMOS mold semiconductor device by the 7th example of this invention.
[Drawing 17] It is a sectional view for explaining the manufacture approach of the semiconductor laser by the 8th example of this invention.
[Description of Notations]
1 Single Crystal Si Substrate
2 Porosity Si Layer

3 P+ Mold Si Layer
4 41 p mold Si layer
5 N+ Mold Si Layer
6 23 Protective coat
7 Oxide Film
9, 11, 15, 19, 21 Adhesives
10 12 Fixture
14 Glass Substrate
16 Light-receiving Side Electrode
18 22 Plastic plate

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
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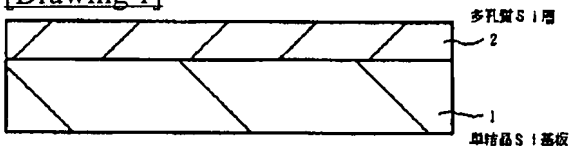
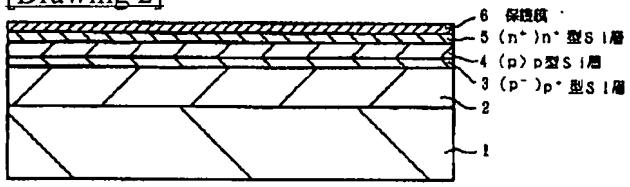
DRAWINGS

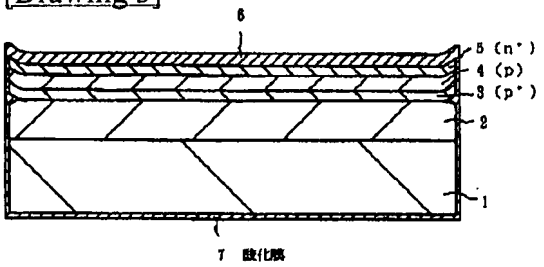
[Drawing 1]



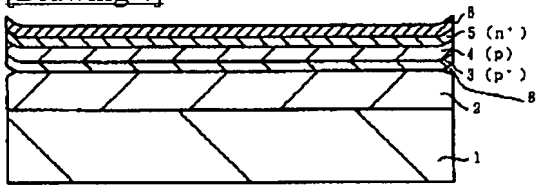
[Drawing 2]



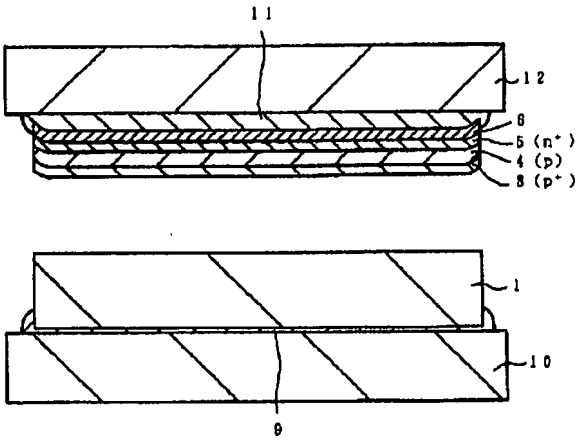
[Drawing 3]



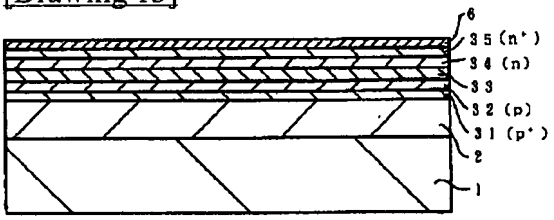
[Drawing 4]



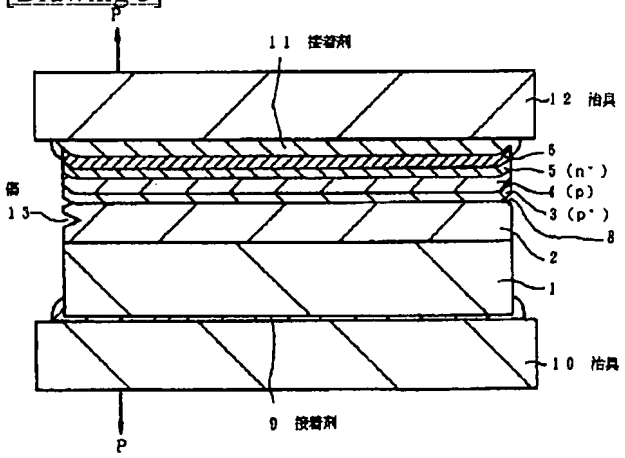
[Drawing 7]



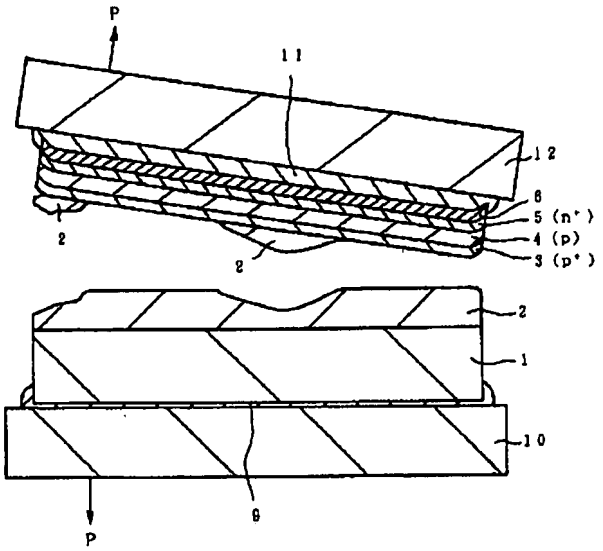
[Drawing 13]



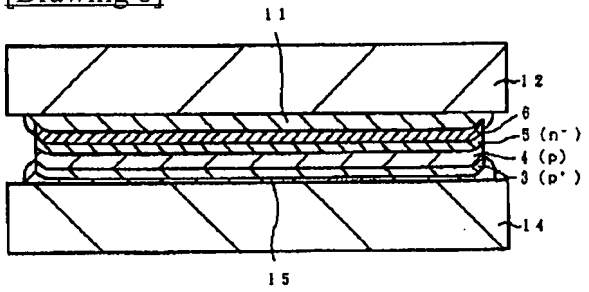
[Drawing 5]



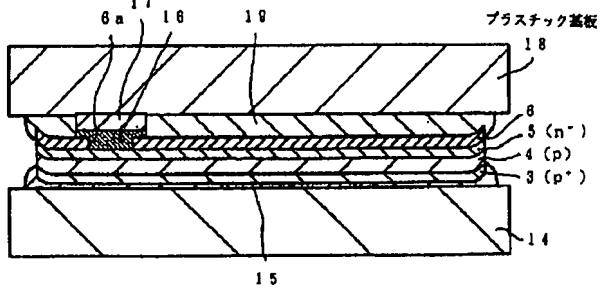
[Drawing 6]



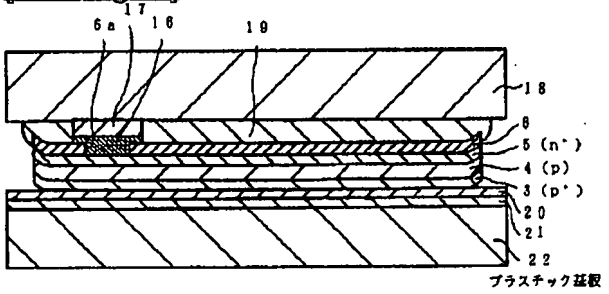
[Drawing 8]



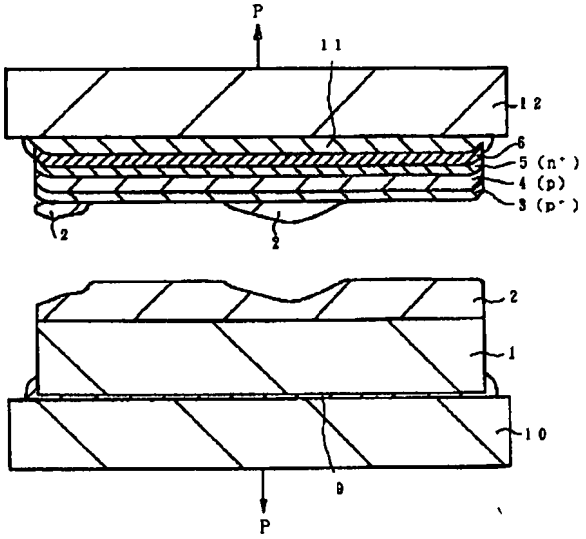
[Drawing 9]



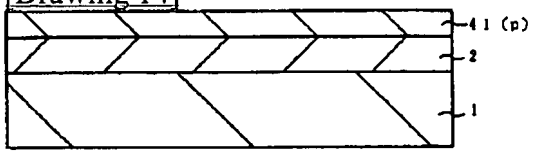
[Drawing 10]



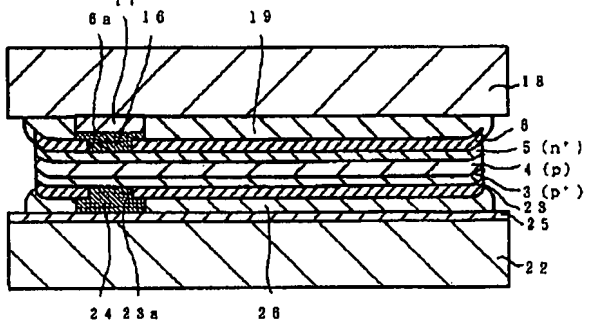
[Drawing 11]



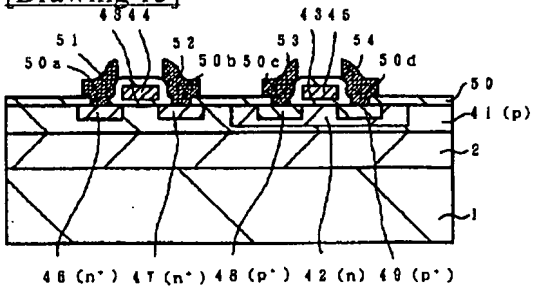
[Drawing 14]



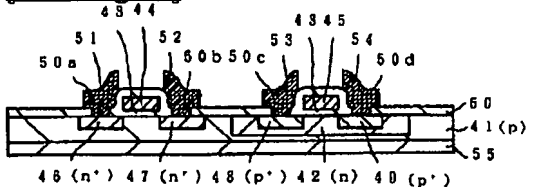
[Drawing 12]



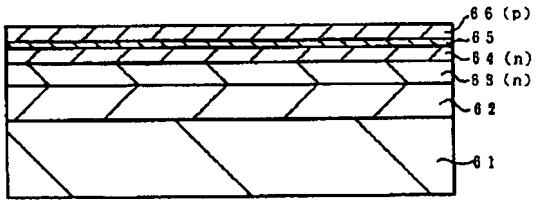
[Drawing 15]



[Drawing 16]



[Drawing 17]



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CORRECTION OR AMENDMENT

[Kind of official gazette] Printing of amendment by the convention of 2 of Article 17 of Patent Law
[Section partition] The 2nd partition of the 7th section
[Publication date] September 14, Heisei 13 (2001. 9.14)

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[Application number] Japanese Patent Application No. 7-37655
[The 7th edition of International Patent Classification]

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H01S 5/30

[FI]

H01L 31/04 H
27/12 F
H01S 3/18
H01L 27/08 321 B
29/78 613 A
31/04 E

[Procedure revision]
[Filing Date] November 8, Heisei 12 (2000. 11.8)
[Procedure amendment 1]
[Document to be Amended] Specification
[Item(s) to be Amended] The name of invention
[Method of Amendment] Modification
[Proposed Amendment]
[Title of the Invention] The approach of separating a semi-conductor layer from a base, the manufacture approach of a semiconductor device, and the manufacture approach of a SOI substrate
[Procedure amendment 2]
[Document to be Amended] Specification
[Item(s) to be Amended] Claim
[Method of Amendment] Modification
[Proposed Amendment]

[Claim(s)]
[Claim 1] The process which forms a porous layer in a base,
It is said base H2 Process which anneals,
The process which forms a semi-conductor layer on said base front face,
It has the process which separates said semi-conductor layer from said base.
How to separate a semi-conductor layer from the base characterized by things.
[Claim 2] Said porous layer is the approach of separating a semi-conductor layer from the base according to claim 1 characterized by forming by anodization.
[Claim 3] Said base is the approach of separating a semi-conductor layer from the base according to claim 1 characterized by consisting of a single crystal.
[Claim 4] Said base is the approach of separating a semi-conductor layer from the base according to claim 1 characterized by consisting of polycrystal.
[Claim 5] Said base is the approach of separating a semi-conductor layer from the base according to claim 1 characterized by consisting of single crystal silicon.
[Claim 6] Said base is the approach of separating a semi-conductor layer from the base according to claim 1 characterized by consisting of a single crystal GaAs.
[Claim 7] Said semi-conductor layer is the approach of separating a semi-conductor layer from the base according to claim 1 characterized by consisting of a silicon layer.
[Claim 8] Said semi-conductor layer is the approach of separating a semi-conductor layer from the base according to claim 1 characterized by consisting of a GaAs layer.
[Claim 9] Said semi-conductor layer is the approach of separating a semi-conductor layer from the base according to claim 1 characterized by consisting of an Si1-x Gex layer ($0< x<=1$).
[Claim 10] How to separate a semi-conductor layer from the base according to claim 1 characterized by having further the process which forms a BAZU beak in said base side face by oxidizing said base thermally before the process which separates said semi-conductor layer.
[Claim 11] How to separate a semi-conductor layer from the base according to claim 1 characterized by having further the process which pastes up a plastic plate on said base of said semi-conductor layer, and the front face of the opposite side before the process which separates said semi-conductor layer.
[Claim 12] How to separate a semi-conductor layer from the base according to claim 1 characterized by having further the process which forms a protective coat on said semi-conductor layer after the process which forms said semi-conductor layer.
[Claim 13] How to separate a semi-conductor layer from the base according to claim 1 characterized by having further the process which removes said porous layer left behind to said semi-conductor layer after the process which separates a semi-conductor layer from said base.
[Claim 14] How to separate a semi-conductor layer from the base according to claim 1 characterized by having further the process which removes said porous layer left behind to said base after the process which separates a semi-conductor layer from said base.
[Claim 15] How to separate a semi-conductor layer from the base according to claim 1 characterized by having further the process which gives a blemish by the laser beam on the side face of said porous layer before the process which separates a semi-conductor layer from said base.
[Claim 16] The process which separates a semi-conductor layer from said base is the approach of separating a semi-conductor layer from the base according to claim 1 characterized by being carried out by making fracture causing mechanically by the interface with the interior of said porous layer and/or said porous layer, said base, and said semi-conductor layer.
[Claim 17] The porosity of said porous layer is the approach of separating a semi-conductor layer from the base according to claim 1 characterized by being 10 - 50%.
[Claim 18] The thickness of said porous layer is the approach of separating a semi-conductor layer from the base according to claim 1 characterized by being 5-50 micrometers.
[Claim 19] The process which forms a porous layer in a base,
It is said base H2 Process which anneals,
The process which forms the semi-conductor layer which constitutes a semiconductor device on said

base front face,
It has the process which separates said semi-conductor layer from said base.
The manufacture approach of the semiconductor device characterized by things.
[Claim 20] Said porous layer is the manufacture approach of the semiconductor device according to claim 19 characterized by forming by anodization.
[Claim 21] Said base is the manufacture approach of the semiconductor device according to claim 19 characterized by consisting of a single crystal.
[Claim 22] Said base is the manufacture approach of the semiconductor device according to claim 19 characterized by consisting of polycrystal.
[Claim 23] Said base is the manufacture approach of the semiconductor device according to claim 19 characterized by consisting of single crystal silicon.
[Claim 24] Said base is the manufacture approach of the semiconductor device according to claim 19 characterized by consisting of a single crystal GaAs.
[Claim 25] Said semi-conductor layer is the manufacture approach of the semiconductor device according to claim 19 characterized by consisting of a silicon layer.
[Claim 26] Said semi-conductor layer is the manufacture approach of the semiconductor device according to claim 19 characterized by consisting of a GaAs layer.
[Claim 27] Said semi-conductor layer is the manufacture approach of the semiconductor device according to claim 19 characterized by consisting of an Si1-x Gex layer (0< x<=1).
[Claim 28] The manufacture approach of the semiconductor device according to claim 19 characterized by having further the process which forms a BAZU beak in said base side face by oxidizing said base thermally before the process which separates said semi-conductor layer.
[Claim 29] The manufacture approach of the semiconductor device according to claim 19 characterized by having further the process which pastes up a plastic plate before the process which separates said semi-conductor layer on said base of said semi-conductor layer, and the front face of the opposite side.
[Claim 30] The manufacture approach of the semiconductor device according to claim 19 characterized by having further the process which forms a protective coat on said semi-conductor layer after the process which forms said semi-conductor layer.
[Claim 31] The manufacture approach of the semiconductor device according to claim 19 characterized by having further the process which removes said porous layer left behind to said semi-conductor layer after the process which separates a semi-conductor layer from said base.
[Claim 32] The manufacture approach of the semiconductor device according to claim 19 characterized by having further the process which removes said porous layer left behind to said base after the process which separates a semi-conductor layer from said base.
[Claim 33] The manufacture approach of the semiconductor device according to claim 19 characterized by having further the process which gives a blemish by the laser beam on the side face of said porous layer before the process which separates a semi-conductor layer from said base.
[Claim 34] The process which separates a semi-conductor layer from said base is the manufacture approach of the semiconductor device according to claim 19 characterized by being carried out by making fracture cause mechanically by the interface with the interior of said porous layer and/or said porous layer, said base, and said semi-conductor layer.
[Claim 35] The porosity of said porous layer is the manufacture approach of the semiconductor device according to claim 19 characterized by being 10 - 50%.
[Claim 36] The thickness of said porous layer is the manufacture approach of the semiconductor device according to claim 19 characterized by being 5-50 micrometers.
[Claim 37] The process which forms a porous layer in a base,
It is said base H2 Process which anneals,
The process which forms a semi-conductor layer on said base front face,
It has the process which separates said semi-conductor layer from said base.
The manufacture approach of the SOI substrate characterized by things.
[Claim 38] Said porous layer is the manufacture approach of the SOI substrate according to claim 37

characterized by forming by anodization.
[Claim 39] Said base is the manufacture approach of the SOI substrate according to claim 37 characterized by consisting of a single crystal.
[Claim 40] Said base is the manufacture approach of the SOI substrate according to claim 37 characterized by consisting of polycrystal.
[Claim 41] Said base is the manufacture approach of the SOI substrate according to claim 37 characterized by consisting of single crystal silicon.
[Claim 42] Said base is the manufacture approach of the SOI substrate according to claim 37 characterized by consisting of a single crystal GaAs.
[Claim 43] Said semi-conductor layer is the manufacture approach of the SOI substrate according to claim 37 characterized by consisting of a silicon layer.
[Claim 44] Said semi-conductor layer is the manufacture approach of the SOI substrate according to claim 37 characterized by consisting of a GaAs layer.
[Claim 45] Said semi-conductor layer is the manufacture approach of the SOI substrate according to claim 37 characterized by consisting of an Si1-x Gex layer (0< x<=1).
[Claim 46] The manufacture approach of the SOI substrate according to claim 37 characterized by having further the process which forms a BAZU beak in said base side face by oxidizing said base thermally before the process which separates said semi-conductor layer.
[Claim 47] The manufacture approach of the SOI substrate according to claim 37 characterized by having further the process which pastes up a plastic plate before the process which separates said semi-conductor layer on said base of said semi-conductor layer, and the front face of the opposite side.
[Claim 48] The manufacture approach of the SOI substrate according to claim 37 characterized by having further the process which forms a protective coat on said semi-conductor layer after the process which forms said semi-conductor layer.
[Claim 49] The manufacture approach of the SOI substrate according to claim 37 characterized by having further the process which removes said porous layer left behind to said semi-conductor layer after the process which separates a semi-conductor layer from said base.
[Claim 50] The manufacture approach of the SOI substrate according to claim 37 characterized by having further the process which removes said porous layer left behind to said base after the process which separates a semi-conductor layer from said base.
[Claim 51] The manufacture approach of the SOI substrate according to claim 37 characterized by having further the process which gives a blemish by the laser beam on the side face of said porous layer before the process which separates a semi-conductor layer from said base.
[Claim 52] The process which separates a semi-conductor layer from said base is the manufacture approach of the SOI substrate according to claim 37 characterized by being carried out by making fracture cause mechanically by the interface with the interior of said porous layer and/or said porous layer, said base, and said semi-conductor layer.
[Claim 53] The porosity of said porous layer is the manufacture approach of the SOI substrate according to claim 37 characterized by being 10 - 50%.
[Claim 54] The thickness of said porous layer is the manufacture approach of the SOI substrate according to claim 37 characterized by being 5-50 micrometers.
[Claim 55] The process which forms a porous layer in a base,
The process which forms a semi-conductor layer on said base front face,
The process which forms a BAZU beak in said base side face by oxidizing said base thermally,
It has the process which separates said semi-conductor layer from said base.
How to separate a semi-conductor layer from the base characterized by things.
[Claim 56] Said porous layer is the approach of separating a semi-conductor layer from the base according to claim 55 characterized by forming by anodization.
[Claim 57] Said base is the approach of separating a semi-conductor layer from the base according to claim 55 characterized by consisting of a single crystal.
[Claim 58] Said base is the approach of separating a semi-conductor layer from the base according to

claim 55 characterized by consisting of polycrystal.
[Claim 59] Said base is the approach of separating a semi-conductor layer from the base according to claim 55 characterized by consisting of single crystal silicon.
[Claim 60] Said base is the approach of separating a semi-conductor layer from the base according to claim 55 characterized by consisting of a single crystal GaAs.
[Claim 61] Said semi-conductor layer is the approach of separating a semi-conductor layer from the base according to claim 55 characterized by consisting of a silicon layer.
[Claim 62] Said semi-conductor layer is the approach of separating a semi-conductor layer from the base according to claim 55 characterized by consisting of a GaAs layer.
[Claim 63] Said semi-conductor layer is the approach of separating a semi-conductor layer from the base according to claim 55 characterized by consisting of an Si1-x Gex layer (0< x<=1).
[Claim 64] How to separate a semi-conductor layer from the base according to claim 55 characterized by having further the process which pastes up a plastic plate on said base of said semi-conductor layer, and the front face of the opposite side before the process which separates said semi-conductor layer.
[Claim 65] How to separate a semi-conductor layer from the base according to claim 55 characterized by having further the process which forms a protective coat on said semi-conductor layer after the process which forms said semi-conductor layer.
[Claim 66] How to separate a semi-conductor layer from the base according to claim 55 characterized by having further the process which removes said porous layer left behind to said semi-conductor layer after the process which separates a semi-conductor layer from said base.
[Claim 67] How to separate a semi-conductor layer from the base according to claim 55 characterized by having further the process which removes said porous layer left behind to said base after the process which separates a semi-conductor layer from said base.
[Claim 68] How to separate a semi-conductor layer from the base according to claim 55 characterized by having further the process which gives a blemish by the laser beam on the side face of said porous layer before the process which separates a semi-conductor layer from said base.
[Claim 69] The process which separates a semi-conductor layer from said base is the approach of separating a semi-conductor layer from the base according to claim 55 characterized by being carried out by making fracture causing mechanically by the interface with the interior of said porous layer and/or said porous layer, said base, and said semi-conductor layer.
[Claim 70] The porosity of said porous layer is the approach of separating a semi-conductor layer from the base according to claim 55 characterized by being 10 - 50%.
[Claim 71] The thickness of said porous layer is the approach of separating a semi-conductor layer from the base according to claim 55 characterized by being 5-50 micrometers.
[Procedure amendment 3]
[Document to be Amended] Specification
[Item(s) to be Amended] 0001
[Method of Amendment] Modification
[Proposed Amendment]
[0001]
[Industrial Application] This invention applies to manufacture of a thin film solar cell, concerning the approach of separating a semi-conductor layer from a base, the manufacture approach of a semiconductor device, and the manufacture approach of a SOI substrate, and is suitable.
[Procedure amendment 4]
[Document to be Amended] Specification
[Item(s) to be Amended] 0007
[Method of Amendment] Modification
[Proposed Amendment]
[0007] That is, the purpose of this invention is to offer the approach of separating a semi-conductor layer from the base which can manufacture the thin film of high performance, such as a thin film solar cell of high conversion efficiency, by low cost, the manufacture approach of a semiconductor device, and the

manufacture approach of a SOI substrate.
[Procedure amendment 5]
[Document to be Amended] Specification
[Item(s) to be Amended] 0008
[Method of Amendment] Modification
[Proposed Amendment]
[0008]
[Means for Solving the Problem] The approach of separating a semi-conductor layer from the base by this invention in order to attain the above-mentioned purpose is [the process which forms a porous layer in a base, and] said base H2 It is characterized by having the process which anneals, the process which forms a semi-conductor layer on said base front face, and the process which separates said semi-conductor layer from said base. The manufacture approach of the semiconductor device by this invention is [the process which forms a porous layer in a base, and] said base H2 It is characterized by having the process which anneals, the process which forms the semi-conductor layer which constitutes a semiconductor device on said base front face, and the process which separates said semi-conductor layer from said base. The manufacture approach of the SOI substrate by this invention is [the process which forms a porous layer in a base, and] said base H2 It is characterized by having the process which anneals, the process which forms a semi-conductor layer on said base front face, and the process which separates said semi-conductor layer from said base. The approach of separating a semi-conductor layer from the base by this further invention is characterized by having the process which forms a porous layer in a base, the process which forms a semi-conductor layer on said base front face, the process which forms a BAZU beak in said base side face by oxidizing said base thermally, and the process which separates said semi-conductor layer from said base.

[Translation done.]

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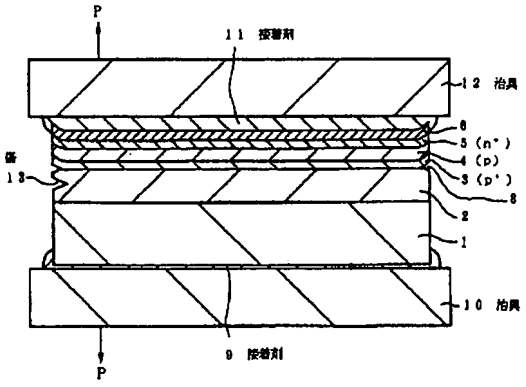
(54)【発明の名称】　基体から素子形成層を分離する方法

(57)【要約】

【目的】　高変換効率の薄膜太陽電池などの高性能の薄膜素子を低コストで製造することができる基体から素子形成層を分離する方法を提供する。

【構成】　単結晶Ｓｉ基板１上に多孔質Ｓｉ層２を形成し、その上に太陽電池層となるｐ$^+$型Ｓｉ層３、ｐ型Ｓｉ層４およびｎ$^+$型Ｓｉ層５を形成する。ｎ$^+$型Ｓｉ層５上に保護膜６を形成した後、単結晶Ｓｉ基板１の裏面を治具１０に接着するとともに、保護膜６の表面に治具１２を接着する。次に、治具１０、１２を互いに反対方向に引っ張ることにより多孔質Ｓｉ層２を機械的に破断し、太陽電池層を単結晶Ｓｉ基板１から分離する。この太陽電池層を二枚のプラスチック基板の間にはさんでフレキシブルな薄膜太陽電池を製造する。



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【特許請求の範囲】

【請求項１】　基体上に分離層を介して素子形成層を形成し、その後上記分離層の内部および／または上記分離層と上記素子形成層および上記基体との界面で機械的に破断を起こさせることにより上記基体から上記素子形成層を分離するようにしたことを特徴とする基体から素子形成層を分離する方法。

【請求項２】　上記分離層の機械的強度は上記基体および上記素子形成層の機械的強度よりも弱いことを特徴とする請求項１記載の基体から素子形成層を分離する方法。

【請求項３】　上記分離層は多孔質であることを特徴とする請求項１記載の基体から素子形成層を分離する方法。

【請求項４】　上記分離層は多結晶であることを特徴とする請求項１記載の基体から素子形成層を分離する方法。

【請求項５】　上記分離層は非晶質であることを特徴とする請求項１記載の基体から素子形成層を分離する方法。

【請求項６】　上記分離層は半導体からなることを特徴とする請求項１記載の基体から素子形成層を分離する方法。

【請求項７】　上記分離層はシリコンからなることを特徴とする請求項１記載の基体から素子形成層を分離する方法。

【請求項８】　上記基体は単結晶であることを特徴とする請求項１記載の基体から素子形成層を分離する方法。

【請求項９】　上記基体は多結晶であることを特徴とする請求項１記載の基体から素子形成層を分離する方法。

【請求項１０】　上記基体は単結晶シリコンからなることを特徴とする請求項１記載の基体から素子形成層を分離する方法。

【請求項１１】　上記基体はキャスト多結晶シリコンからなることを特徴とする請求項１記載の基体から素子形成層を分離する方法。

【請求項１２】　上記素子形成層は半導体からなることを特徴とする請求項１記載の基体から素子形成層を分離する方法。

【請求項１３】　上記素子形成層は単結晶シリコンからなることを特徴とする請求項１記載の基体から素子形成層を分離する方法。

【請求項１４】　上記基体と上記素子形成層とを互いに反対方向に引っ張ることにより上記分離層の内部および／または上記分離層と上記素子形成層および上記基体との界面で機械的に破断を起こさせるようにしたことを特徴とする請求項１記載の基体から素子形成層を分離する方法。

【請求項１５】　上記基体の上記分離層と反対側の主面を第１の治具に接着するとともに、上記素子形成層の上

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記分離層と反対側の主面を第２の治具に接着し、上記第１の治具および上記第２の治具を互いに反対方向に引っ張ることにより上記分離層の内部および／または上記分離層と上記素子形成層および上記基体との界面で機械的に破断を起こさせるようにしたことを特徴とする請求項１記載の基体から素子形成層を分離する方法。

【請求項１６】　単結晶シリコンからなる上記基体を陽極化成することにより多孔質シリコンからなる上記分離層を形成し、上記分離層上に単結晶シリコンからなる上記素子形成層を形成するようにしたことを特徴とする請求項１記載の基体から素子形成層を分離する方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】この発明は、基体から素子形成層を分離する方法に関し、例えば、薄膜太陽電池の製造に適用して好適なものである。

【０００２】

【従来の技術】太陽電池が発明されてから約４０年が経過した。太陽電池は一部実用化されてはいるものの、本格的に使用されるためには、特に低コスト化が重要である。また、地球環境の温暖化を防ぐという意味においては、エネルギー回収年数が例えば１年以下になる必要がある。したがって、太陽電池の製造に要するエネルギーを極力低減するため、製造に多くのエネルギーを要する厚膜太陽電池よりも薄膜太陽電池の方が望ましいことになる。

【０００３】一方、薄膜太陽電池はある程度折り曲げることが可能であるため、例えば自動車のボディーの曲面部やポータブル電気製品の外部の曲面部に搭載して発電を行うことができる。あるいは、この薄膜太陽電池をソーラー充電器に応用した場合には、薄膜太陽電池を使用するときは広げ、使用しないときは折り畳むということも可能になる。

【０００４】従来、このような薄膜太陽電池として、プラスチック基板上に形成したアモルファスシリコン太陽電池がある。ところが、このアモルファスシリコン太陽電池は、光電変換の変換効率が低い上に使用中に変換効率が低下するという問題がある。このため、アモルファスシリコンに比べて変換効率が高い単結晶シリコンまたは多結晶シリコンを用いた薄膜太陽電池の実現が望まれていた。

【０００５】

【発明が解決しようとする課題】しかしながら、単結晶シリコンまたは多結晶シリコンを形成するプロセス温度はかなり高いため、プラスチック基板やガラス基板上に形成することは困難であった。

【０００６】この発明は、従来技術が有する上述の問題を解決するものである。

【０００７】すなわち、この発明の目的は、高変換効率の薄膜太陽電池などの高性能の薄膜素子を低コストで製

造することができる基体から素子形成層を分離する方法を提供することにある。

【０００８】

【課題を解決するための手段】上記目的を達成するために、この発明による基体から素子形成層を分離する方法は、基体上に分離層を介して素子形成層を形成し、その後分離層の内部および／または分離層と素子形成層および基体との界面で機械的に破断を起こさせることにより基体から素子形成層を分離するようにしたことを特徴とするものである。

【０００９】この発明において、典型的には、分離層の機械的強度は基体および素子形成層の機械的強度よりも弱い。

【００１０】この発明において、分離層は、例えば多孔質、多結晶または非晶質である。

【００１１】この発明において、典型的には、分離層は半導体からなる。この半導体は、元素半導体であっても、化合物半導体であってもよい。前者の一例はシリコン（Ｓｉ）であり、後者の一例はヒ化ガリウム（ＧａＡｓ）である。

【００１２】この発明において、好適には、基体は単結晶であるが、多結晶でもよい。

【００１３】この発明において、好適には、基体は単結晶シリコンからなるが、例えばキャスト多結晶シリコンからなるものでもよい。

【００１４】この発明において、典型的には、素子形成層は半導体からなる。この場合、素子は半導体素子である。

【００１５】この発明の好適な一実施形態においては、素子形成層は単結晶シリコンからなる。

【００１６】この発明においては、典型的には、基体と素子形成層とを互いに反対方向に引っ張ることにより分離層の内部および／または分離層と素子形成層および基体との界面で機械的に破断を起こさせる。より実際的には、基体の分離層と反対側の主面を第１の治具に接着するとともに、素子形成層の分離層と反対側の主面を第２の治具に接着し、第１の治具および第２の治具を互いに反対方向に引っ張ることにより分離層の内部および／または分離層と素子形成層および基体との界面で機械的に破断を起こさせる。

【００１７】この発明の典型的な一実施形態においては、単結晶シリコンからなる基体を陽極化成することにより多孔質シリコンからなる分離層を形成し、分離層上に単結晶シリコンからなる素子形成層を形成する。

【００１８】この発明においては、典型的には、分離層の機械的な破断を行った後に基体上に残された分離層は研磨および／またはエッチングにより除去し、素子形成層の裏面に残された分離層も同様に研磨および／またはエッチングにより除去する。このようにして分離された基体は再び使用される。ここで、例えば、陽極化成などのような基体の厚さが減少するプロセスを用いて分離層を形成する場合には、その厚さの減少を補うために、基体上にこの基体と同一の物質を成長させて元の厚さに復元するようにすればよい。

【００１９】この発明において、素子形成層は各種の素子に用いられるものであってよく、その一例を挙げると、薄膜太陽電池における太陽電池層である。

【００２０】

【作用】上述のように構成されたこの発明によれば、分離層の内部および／または分離層と素子形成層および基体との界面で機械的に破断を起こさせることにより基体から素子形成層を分離するようにしているので、この素子形成層を薄膜に形成しておくことにより、この薄膜の素子形成層を用いて薄膜素子、例えば薄膜太陽電池を製造することができる。この場合、素子形成層が薄膜であることや、素子形成層を分離するために基体の研磨やエッチングなどを行わないので基体を繰り返し使用することができることなどにより、薄膜素子、例えば薄膜太陽電池を低コストで製造することができる。さらに、素子形成層を単結晶または多結晶に形成することにより、高性能の薄膜素子、特に薄膜太陽電池にあっては高変換効率のものを得ることができる。また、この薄膜素子、例えば薄膜太陽電池はある程度折り曲げることが可能であるので、フレキシブルな薄膜素子、例えばフレキシブルな薄膜太陽電池を得ることができる。

【００２１】

【実施例】以下、この発明の実施例について図面を参照しながら説明する。なお、実施例の全図において、同一または対応する部分には同一の符号を付す。

【００２２】図１～図１０はこの発明の第１実施例による薄膜太陽電池の製造方法を工程順に示す断面図である。

【００２３】この第１実施例による薄膜太陽電池の製造方法においては、まず、図１に示すように、単結晶Ｓｉ基板１を陽極化成（陽極酸化）することにより多孔質Ｓｉ層２を形成する。この陽極化成法による多孔質Ｓｉ層２の形成方法はよく知られており（例えば、応用物理第５７巻、第１１号、第１７１０頁（１９８８））、例えば、電流密度を３０ｍＡとし、陽極化成溶液として$HF : H_2O : C_2H_5OH = 1 : 1 : 1$を用いた場合、得られる多孔質Ｓｉ層２の厚さは５～５０μｍ、多孔度（porosity）は１０～５０％である。この多孔質Ｓｉ層２の厚さは、単結晶Ｓｉ基板１を繰り返し使用する観点からは、この単結晶Ｓｉ基板１の厚さの減少を少なくし、使用可能回数を多くするために、可能な限り薄くすることが望ましく、好適には５～１５μｍ、例えば約１０μｍに選ばれる。また、単結晶Ｓｉ基板１は、陽極化成によりその上に多孔質Ｓｉ層２を形成する観点からはｐ型であることが望ましいが、ｎ型であっても、条件設定によっては多孔質Ｓｉ層２を形成することが可能であ

る。

【００２４】次に、図２に示すように、多孔質Ｓｉ層２上に例えばＣＶＤ法により例えば７００～１１００℃の温度でp^+型Ｓｉ層３、ｐ型Ｓｉ層４およびn^+型Ｓｉ層５を順次エピタキシャル成長させた後、n^+型Ｓｉ層５上に例えばＣＶＤ法により例えば単層のSiO_2膜やＳｉＮ膜あるいはそれらの積層膜からなる保護膜６を形成する。ここで、p^+型Ｓｉ層３、ｐ型Ｓｉ層４およびn^+型Ｓｉ層５は太陽電池層を構成し、それらの合計の厚さは典型的には１～５０μｍ、例えば５μｍである。また、この場合、太陽電池層を構成するこれらのp^+型Ｓｉ層３、ｐ型Ｓｉ層４およびn^+型Ｓｉ層５の結晶性を良好にするため、それらのエピタキシャル成長前に、多孔質Ｓｉ層２を例えば４００～６００℃の温度で短時間酸化することによりその内部の孔の内壁に薄い酸化膜を形成してその強度を高めるとともに、例えば真空中において例えば９５０～１０００℃の温度でH_2アニールすることにより多孔質Ｓｉ層２の表面の孔を極力埋めておき、エピタキシャル成長が良好に行われるようにするのが好ましい。このようにすることにより、単結晶のp^+型Ｓｉ層３、ｐ型Ｓｉ層４およびn^+型Ｓｉ層５を得ることができる（例えば、日経マイクロデバイス、１９９４年７月号、第７６頁）。

【００２５】次に、図３に示すように、上述のように多孔質Ｓｉ層２、p^+型Ｓｉ層３、ｐ型Ｓｉ層４、n^+型Ｓｉ層５および保護膜６が形成された単結晶Ｓｉ基板１の全体を熱酸化することにより、その表面全体に例えば膜厚が５０～５００ｎｍのSiO_2膜からなる酸化膜７を形成する。この熱酸化時には、多孔質Ｓｉ層２の酸化速度が単結晶Ｓｉ基板１の酸化速度よりも速く、また、多孔質Ｓｉ層２の体積が膨張するため、エッジ部における多孔質Ｓｉ層２とp^+型Ｓｉ層３との界面に酸化膜７がバーズビーク状に形成され、エッジ部におけるp^+型Ｓｉ層３、ｐ型Ｓｉ層４、n^+型Ｓｉ層５および保護膜６の全体が持ち上がった構造となる。

【００２６】次に、酸化膜７をエッチング除去する。これによって、図４に示すように、エッジ部における多孔質Ｓｉ層２とp^+型Ｓｉ層３との間に楔状の間隙８が形成される。この楔状の間隙８は、後の工程で多孔質Ｓｉ層２の引っ張りによる破断を容易に行うことができるようにするためのものである。

【００２７】次に、図５に示すように、単結晶Ｓｉ基板１の裏面を接着剤９により治具１０に接着するとともに、保護膜６の表面に接着剤１１によりもう一つの治具１２を接着する。これらの治具１０、１２は、後の工程で行われる引っ張りに耐えられるだけの十分な強度を有するものが用いられ、例えば金属や石英などからなるものが用いられる。また、接着剤９、１１は、後の工程で行われる引っ張りに耐えられるだけの十分な接着強度を有するものが用いられ、例えば瞬間接着剤などが用いられる。さらに、この場合、後の工程で多孔質Ｓｉ層２の引っ張りによる破断をより容易に行うことができるようにするため、多孔質Ｓｉ層２のエッジ部の側壁にあらかじめ傷１３を付けておく。この傷１３は、機械的な方法で付けることができるほか、レーザービームの照射などによって付けることもできる。

【００２８】次に、図５に示すように、治具１０、１２に十分に大きな外力Ｐを加えて引っ張る。このとき、この外力Ｐは、単結晶Ｓｉ基板１の中心から多孔質Ｓｉ層２の傷１３が付いているエッジ部側にずれた位置に加え、多孔質Ｓｉ層２のエッジ部に応力集中が起きるようにする。この結果、多孔質Ｓｉ層２はそれ自身機械的強度が低いことに加えて、多孔質Ｓｉ層２のエッジ部の側壁にあらかじめ傷１３が付いていることやエッジ部における多孔質Ｓｉ層２とp^+型Ｓｉ層３との間に楔状の間隙８が形成されていることによりこれらの場所で応力集中が極めて顕著に起き、図６に示すように、多孔質Ｓｉ層２の内部や多孔質Ｓｉ層２とp^+型Ｓｉ層３との界面で破断が起きる。これによって、単結晶Ｓｉ基板１と、p^+型Ｓｉ層３、ｐ型Ｓｉ層４、n^+型Ｓｉ層５および保護膜６とが互いに分離される。

【００２９】次に、図７に示すように、上述の破断後に単結晶Ｓｉ基板１の表面およびp^+型Ｓｉ層３の表面にそれぞれ残された多孔質Ｓｉ層２を例えばHF/H_2O_2のようなエッチング液を用いてエッチング除去する。単結晶Ｓｉ基板１は、接着剤９を除去し、治具１０を取り外した後、その表面を研磨して再び薄膜太陽電池製造用の基板として用いられる。ここで、例えば、多孔質Ｓｉ層２の厚さを１０μｍ、単結晶Ｓｉ基板１を再使用するための研磨により除去される厚さが３μｍ程度であるとすると、薄膜太陽電池の製造の１サイクルで減少する単結晶Ｓｉ基板１の厚さは１３μｍである。したがって、単結晶Ｓｉ基板１を１０回使用しても、単結晶Ｓｉ基板１の厚さの減少は１３０μｍに過ぎないため、通常は単結晶Ｓｉ基板１を少なくとも１０回は使用することが可能である。

【００３０】次に、図８に示すように、p^+型Ｓｉ層３の露出した表面を例えばガラス基板１４の表面に接着剤１５により接着する。この接着剤１５としては例えばエポキシ樹脂系のものが用いられる。

【００３１】次に、接着剤１１を除去して保護膜６から治具１２を取り外した後、図９に示すように、保護膜６の所定部分をエッチング除去して開口６ａを形成し、この開口６ａを通じてn^+型Ｓｉ層５上に受光面電極１６を形成する。この受光面電極１６は、例えば印刷法により形成する。この後、この受光面電極１６に対応する部分にこの受光面電極１６と同一形状の金属層１６があらかじめ形成されたプラスチック基板１８を用意し、これらの受光面電極１６および金属層１７同士を接続する。このとき、保護膜６とプラスチック基板１８との間には

隙間が形成されるので、この隙間に例えばエポキシ樹脂系の透明な接着剤１９を充填して保護膜６とプラスチック基板１８とを接着する。

【００３２】次に、接着剤１５を除去してp^+型Ｓｉ層３からガラス基板１４を取り外した後、図１０に示すように、例えば印刷法によりp^+型Ｓｉ層３上に裏面電極２０を形成し、この裏面電極２０に接着剤２１によりプラスチック基板２２を接着する。ここで、この裏面電極２０は、薄膜太陽電池に対する入射光の反射板ともなり、高変換効率化に寄与する。

【００３３】以上により、太陽電池層を構成するp^+型Ｓｉ層３、ｐ型Ｓｉ層４およびn^+型Ｓｉ層５と保護膜６とが二枚のプラスチック基板１８、２２間にはさまれた構造の目的とする薄膜太陽電池が完成する。

【００３４】以上のように、この第１実施例によれば、単結晶Ｓｉ基板１上に多孔質Ｓｉ層２を介して太陽電池層を構成する単結晶のp^+型Ｓｉ層３、ｐ型Ｓｉ層４およびn^+型Ｓｉ層５を順次エピタキシャル成長させた後、多孔質Ｓｉ層２を引っ張りにより機械的に破断してこの太陽電池層を単結晶Ｓｉ基板１から分離し、この太陽電池層を二枚のプラスチック基板１８、２２間にはさむことにより薄膜太陽電池を製造している。この場合、太陽電池層が単結晶であることにより、この薄膜太陽電池は高変換効率であり、信頼性にも優れている。また、単結晶Ｓｉ基板１を繰り返し使用することができること、単結晶Ｓｉ基板１からの太陽電池層の分離に機械的な方法を用いていること、安価なプラスチック基板１８、２２を用いていることなどにより、この薄膜太陽電池は低コストで製造することができる。また、この薄膜太陽電池は、太陽電池層が薄くてそれ自身ある程度曲げることができることやフレキシブルなプラスチック基板１８、２２を用いていることなどにより、全体としてある程度折り曲げ可能であることから、例えば自動車のボディーの曲面部やポータブル電気製品の外部の曲面部に搭載することができ、応用範囲が広い。

【００３５】すなわち、この第１実施例によれば、高変換効率かつ高信頼性のフレキシブルな薄膜太陽電池を低コストで製造することができる。

【００３６】次に、この発明の第２実施例について説明する。

【００３７】上述の第１実施例による薄膜太陽電池の製造方法においては、多孔質Ｓｉ層２の破断により単結晶Ｓｉ基板１とp^+型Ｓｉ層３、ｐ型Ｓｉ層４、n^+型Ｓｉ層５および絶縁膜６とを分離する際に治具１０、１２に図５に示すように外力Ｐを加えたのに対して、この第２実施例による薄膜太陽電池の製造方法においては、図１１に示すように治具１０、１２に外力Ｐを加えることにより多孔質Ｓｉ層２の破断を行い、単結晶Ｓｉ基板１とp^+型Ｓｉ層３、ｐ型Ｓｉ層４、n^+型Ｓｉ層５および絶縁膜６とを分離する。この第２実施例による薄膜太陽電池の製造方法のその他のことは、第１実施例による薄膜太陽電池の製造方法と同様であるので、説明を省略する。

【００３８】この第２実施例によっても、第１実施例と同様に、高変換効率かつ高信頼性のフレキシブルな薄膜太陽電池を低コストで製造することができる。

【００３９】次に、この発明の第３実施例について説明する。

【００４０】上述の第１実施例による薄膜太陽電池の製造方法においては、図１０に示すように、p^+型Ｓｉ層３の全面が裏面電極２０と接触しているため、このp^+型Ｓｉ層３と裏面電極２０との界面において光入射により発生した電子ー正孔対の再結合が起きやすく、それが変換効率を低下させるおそれがある。そこで、この第３実施例による薄膜太陽電池の製造方法においては、図１２に示すように、p^+型Ｓｉ層３上に単層のSiO_2膜やＳｉＮ膜あるいはそれらの積層膜からなる保護膜２３を形成し、この絶縁膜２３に開口２３ａを形成し、この開口２３ａを通じて例えば印刷法により裏面電極２４を形成し、この裏面電極２４をプラスチック基板２２上にあらかじめ形成された金属層２５と接続する。このとき、保護膜２３と金属層２５との間には隙間が形成されるので、この隙間に例えばエポキシ樹脂系の透明な接着剤２６を充填して保護膜２３と金属層２５とを接着する。この第３実施例による薄膜太陽電池の製造方法のその他のことは、第１実施例による薄膜太陽電池の製造方法と同様であるので、説明を省略する。

【００４１】この第３実施例によれば、p^+型Ｓｉ層３と裏面電極２４との界面における電子ー正孔対の再結合を大幅に減少させることができることにより、薄膜太陽電池の変換効率を第１実施例に比べてより高くすることができるほか、第１実施例と同様な利点がある。

【００４２】次に、この発明の第４実施例について説明する。

【００４３】上述の第１実施例による薄膜太陽電池の製造方法においては、図８に示す工程において一旦太陽電池層の裏面をガラス基板１４に接着し、その後このガラス基板１４を取り外してから、図１０に示す工程においてこの太陽電池層をプラスチック基板２２に接着するようにしているが、この第４実施例による薄膜太陽電池の製造方法においては、太陽電池層をガラス基板１４に接着せず、p^+型Ｓｉ層３に印刷法により直接裏面電極２０を形成し、この裏面電極２０を接着剤２１によりプラスチック基板２２に接着する。この後、接着剤１１を除去して治具１２を取り外し、保護膜６に開口６ａを形成するとともに、受光面電極１６を形成し、この受光面電極１６とプラスチック基板１８上の金属層１７とを接続し、さらに保護膜６とプラスチック基板１８との間の隙間に接着剤１９を充填して接着する。この第４実施例による薄膜太陽電池の製造方法のその他のことは、第１実

施例による薄膜太陽電池の製造方法と同様であるので、説明を省略する。

【００４４】この第４実施例によれば、第１実施例に比べて製造工程の簡略化を図ることができ、したがってより低コストで薄膜太陽電池を製造することができるという利点がある。

【００４５】次に、この発明の第５実施例について説明する。

【００４６】上述の第１実施例による薄膜太陽電池の製造方法においては、図９に示す工程において受光面電極１６を形成したが、この第５実施例による薄膜太陽電池の製造方法においては、図３に示す工程において保護膜６に開口６ａを形成するとともに、受光面電極１６を形成する。この第５実施例による薄膜太陽電池の製造方法のその他のことは、第１実施例による薄膜太陽電池の製造方法と同様であるので、説明を省略する。

【００４７】この第５実施例によっても、第１実施例と同様な利点を得ることができる。

【００４８】次に、この発明の第６実施例について説明する。

【００４９】この第６実施例による薄膜太陽電池の製造方法においては、太陽電池層をダブルヘテロ構造とする。すなわち、この第６実施例においては、図１３に示すように、多孔質Ｓｉ層２上にp^+型Ｓｉ層３１、ｐ型$Si_{1-x}Ge_x$グレーディッド層３２、例えばアンドープの$Si_{1-y}Ge_y$層３３、ｎ型$Si_{1-x}Ge_x$グレーディッド層３４およびn^+型Ｓｉ層３５を順次エピタキシャル成長させ、ダブルヘテロ構造の太陽電池層を形成する。この場合、ｐ型$Si_{1-x}Ge_x$グレーディッド層３２のＧｅ組成比ｘは、このｐ型$Si_{1-x}Ge_x$グレーディッド層３２の厚さ方向に、p^+型Ｓｉ層３１とこのｐ型$Si_{1-x}Ge_x$グレーディッド層３２との界面における０の値から$Si_{1-y}Ge_y$層３３とこのｐ型$Si_{1-x}Ge_x$グレーディッド層３２との界面におけるｙの値まで単調に増加している。また、ｎ型$Si_{1-x}Ge_x$グレーディッド層３４のＧｅ組成比ｘは、このｎ型$Si_{1-x}Ge_x$グレーディッド層３４の厚さ方向に、n^+型Ｓｉ層３５とこのｎ型$Si_{1-x}Ge_x$グレーディッド層３４との界面における０の値から$Si_{1-y}Ge_y$層３３とこのｐ型$Si_{1-x}Ge_x$グレーディッド層３４との界面におけるｙの値まで単調に増加している。これによって、これらのp^+型Ｓｉ層３１、ｐ型$Si_{1-x}Ge_x$グレーディッド層３２、$Si_{1-y}Ge_y$層３３、ｎ型$Si_{1-x}Ge_x$グレーディッド層３４およびn^+型Ｓｉ層３５間の各界面において格子が整合することから、良好な結晶性を得ることができる。この第６実施例による薄膜太陽電池の製造方法のその他のことは第１実施例による薄膜太陽電池の製造方法と同様であるので、説明を省略する。

【００５０】この第６実施例によれば、太陽電池層がダブルヘテロ構造であり、その中央の$Si_{1-y}Ge_y$層３３にキャリアおよび光を有効に閉じ込めることができることにより高い変換効率を得ることができるほか、第１実施例と同様な種々の利点がある。

【００５１】次に、この発明の第７実施例について説明する。この第７実施例は、ＣＭＯＳ型半導体装置の製造にこの発明を適用した実施例である。

【００５２】この第７実施例によるＣＭＯＳ型半導体装置の製造方法においては、まず、図１４に示すように、単結晶Ｓｉ基板１上に多孔質Ｓｉ層２を形成した後、この多孔質Ｓｉ層２上に例えばＣＶＤ法により単結晶のｐ型Ｓｉ層４１をエピタキシャル成長させる。このｐ型Ｓｉ層４１の厚さは必要に応じて選ばれるが、例えば５μｍとする。また、このｐ型Ｓｉ層４１の不純物濃度は例えば$10^{15}cm^{-3}$程度とする。

【００５３】次に、図１５に示すように、このｐ型Ｓｉ層４１中にイオン注入法や熱拡散法によりｎ型不純物を選択的にドープしてｎウエル４２を形成する。次に、ｐ型Ｓｉ層４１上に例えば熱酸化法により例えばSiO_2膜のようなゲート絶縁膜４３を形成した後、このゲート絶縁膜４３上にゲート電極４４、４５を形成する。ここで、これらのゲート電極４４、４５は、例えば、ゲート絶縁膜４３上に例えばＣＶＤ法により多結晶Ｓｉ膜を形成し、この多結晶Ｓｉ膜に不純物をドープして低抵抗化した後、この不純物がドープされた多結晶Ｓｉ膜をエッチングによりパターニングすることにより形成する。

【００５４】次に、ｎウエル４２の部分の表面をマスクで覆った状態でゲート電極４４をマスクとしてｐ型Ｓｉ層４１中にｎ型不純物をイオン注入することにより、ソース領域またはドレイン領域として用いられるn^+型領域４６、４７をゲート電極４４に対して自己整合的に形成する。次に、このｎ型不純物のイオン注入に用いたマスクを除去した後、ｎウエル４２の部分を除いた部分の表面を覆う別のマスクを形成した状態で、ゲート電極４５をマスクとしてｎウエル４２中にｐ型不純物をイオン注入することにより、ソース領域またはドレイン領域として用いられるp^+型領域４８、４９をゲート電極４５に対して自己整合的に形成する。

【００５５】次に、例えばＣＶＤ法により全面に例えばSiO_2膜のような層間絶縁膜５０を形成した後、この層間絶縁膜５０の所定部分をエッチング除去してコンタクトホール５０ａ、５０ｂ、５０ｃ、５０ｄを形成する。次に、例えばスパッタリング法や真空蒸着法により全面に例えばＡｌ膜を形成した後、このＡｌ膜をエッチングによりパターニングして電極５１、５２、５３、５４を形成する。この場合、ゲート電極４４とn^+型領域４６、４７とによりｎチャネルＭＯＳトランジスタが形成され、ゲート電極４５とp^+型領域４８、４９とによりｐチャネルＭＯＳトランジスタが形成される。そして、これらのｎチャネルＭＯＳトランジスタおよびｐチ

ャネルMOSトランジスタによりCMOSが形成される。

【００５６】次に、第１実施例の図５に示すと同様にして、単結晶Ｓｉ基板１の裏面を接着剤９により治具１０に接着するとともに、CMOS型半導体装置の表面に接着剤１１により治具１２を接着する。次に、これらの治具１０、１２に外力Ｐを加えて互いに反対方向に引っ張ることにより多孔質Ｓｉ層２の破断を行い、単結晶Ｓｉ基板１からCMOS型半導体装置を分離する。

【００５７】次に、ｐ型Ｓｉ層４１の裏面から残りの多孔質Ｓｉ層２を除去し、さらに治具１０、１２を取り外した後、図１６に示すように、このｐ型Ｓｉ層４１の裏面を例えば銀ペーストなどにより金属からなるヒートシンク５５とはり合わせる。この後、必要に応じてチップ化（ペレタイズ）を行う。

【００５８】以上により、ｐ型Ｓｉ層４１の裏面にヒートシンク５５を有するCMOS型半導体装置が製造される。

【００５９】この第７実施例によれば、活性層を構成するｐ型Ｓｉ層４１が単結晶であることによりバルクＳｉによるCMOSに匹敵する高い性能を有するCMOS型半導体装置を低コストで製造することができる。また、このCMOS型半導体装置のｐ型Ｓｉ層４１の裏面にはヒートシンク５５が設けられていることにより、動作時の温度上昇を少なくすることができ、温度上昇に伴う性能劣化や不良を防止することができる。

【００６０】次に、この発明の第８実施例について説明する。この第８実施例は、ダブルヘテロ構造の半導体レーザーの製造にこの発明を適用した実施例である。

【００６１】この第８実施例による半導体レーザーの製造方法においては、図１７に示すように、まず、単結晶ＧａＡｓ基板６１上に多孔質ＧａＡｓ層６２を形成する。次に、この多孔質ＧａＡｓ層６２上にｎ型ＧａＡｓ層６３をエピタキシャル成長させ、このｎ型ＧａＡｓ層６３上にｎ型クラッド層としてのｎ型ＡｌＧａＡｓ層６４、ＧａＡｓからなる活性層６５およびｐ型クラッド層としてのｐ型ＡｌＧａＡｓ層６６を順次エピタキシャル成長させてレーザー構造を形成する。なお、ｎ型ＧａＡｓ層６３の厚さは必要に応じて選ばれるが、例えば５μｍとする。

【００６２】次に、第１実施例の図５に示すと同様にして、単結晶ＧａＡｓ基板６１の裏面を接着剤９により治具１０に接着するとともに、ｐ型ＡｌＧａＡｓ層６６の表面に接着剤１１により治具１２を接着する。次に、これらの治具１０、１２に外力Ｐを加えて互いに反対方向に引っ張ることにより多孔質ＧａＡｓ層６２の破断を行い、単結晶ＧａＡｓ基板６１からｎ型ＧａＡｓ層６３、ｎ型ＡｌＧａＡｓ層６４、活性層６５およびｐ型ＡｌＧａＡｓ層６６を分離する。

【００６３】次に、ｎ型ＧａＡｓ層６３の裏面に残された多孔質ＧａＡｓ層６２を除去し、さらに治具１０、１２を取り外した後、図示は省略するが、このｎ型ＧａＡｓ層６３の裏面にｎ側電極を形成するとともに、ｐ型ＡｌＧａＡｓ層６６上にｐ側電極を形成し、目的とするダブルヘテロ構造の半導体レーザーを製造する。

【００６４】この第８実施例によれば、ダブルヘテロ構造の半導体レーザーを低コストで製造することができる。また、この半導体レーザーにおいては、ｎ型ＧａＡｓ層６３が基板の役割を果たすが、このｎ型ＧａＡｓ層６３は半導体レーザーにおいて通常用いられるｎ型ＧａＡｓ基板に比べて非常に薄いので、基板による直列抵抗を極めて小さくすることができ、その分だけ半導体レーザーの動作電圧の低減を図ることができる。

【００６５】以上、この発明の実施例について具体的に説明したが、この発明は、上述の実施例に限定されるものではなく、この発明の技術的思想に基づく各種の変形が可能である。

【００６６】例えば、上述の第１実施例においては、多孔質Ｓｉ層２上にCVD法によってp^+型Ｓｉ層３、ｐ型Ｓｉ層４およびn^+型Ｓｉ層５をエピタキシャル成長させているが、多孔質Ｓｉ層２上にプラズマCVD法などにより非晶質Ｓｉ層を形成し、その後例えば６００～８００℃の温度でアニールを行うことによりこの非晶質Ｓｉ層を固相成長させて結晶化させるようにしてもよい。この場合、多孔質Ｓｉ層２が種結晶となることにより、高品質な固相エピタキシャル層の形成が可能である。

【００６７】また、上述の第６実施例における$Si_{1-y}Ge_y$層３３の代わりに、Ｇｅ層を用いてもよい。

【００６８】さらに、この発明は、例えばSOI（silicon on insulator）基板の製造に適用することも可能である。

【００６９】

【発明の効果】以上説明したように、この発明によれば、分離層の内部および／または分離層と素子形成層および基体との界面で機械的に破断を起こさせることにより基体から素子形成層を分離するようにしているので、例えば高変換効率の薄膜太陽電池などの高性能の薄膜素子を低コストで製造することができる。

【図面の簡単な説明】

【図１】この発明の第１実施例による薄膜太陽電池の製造方法を説明するための断面図である。

【図２】この発明の第１実施例による薄膜太陽電池の製造方法を説明するための断面図である。

【図３】この発明の第１実施例による薄膜太陽電池の製造方法を説明するための断面図である。

【図４】この発明の第１実施例による薄膜太陽電池の製造方法を説明するための断面図である。

【図５】この発明の第１実施例による薄膜太陽電池の製造方法を説明するための断面図である。

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【図６】この発明の第１実施例による薄膜太陽電池の製造方法を説明するための断面図である。

【図７】この発明の第１実施例による薄膜太陽電池の製造方法を説明するための断面図である。

【図８】この発明の第１実施例による薄膜太陽電池の製造方法を説明するための断面図である。

【図９】この発明の第１実施例による薄膜太陽電池の製造方法を説明するための断面図である。

【図１０】この発明の第１実施例による薄膜太陽電池の製造方法を説明するための断面図である。

【図１１】この発明の第２実施例による薄膜太陽電池の製造方法を説明するための断面図である。

【図１２】この発明の第３実施例による薄膜太陽電池の製造方法を説明するための断面図である。

【図１３】この発明の第６実施例による薄膜太陽電池の製造方法を説明するための断面図である。

【図１４】この発明の第７実施例によるＣＭＯＳ型半導体装置の製造方法を説明するための断面図である。

【図１５】この発明の第７実施例によるＣＭＯＳ型半導体装置の製造方法を説明するための断面図である。

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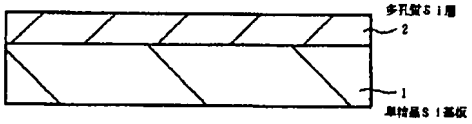
【図１６】この発明の第７実施例によるＣＭＯＳ型半導体装置の製造方法を説明するための断面図である。

【図１７】この発明の第８実施例による半導体レーザーの製造方法を説明するための断面図である。

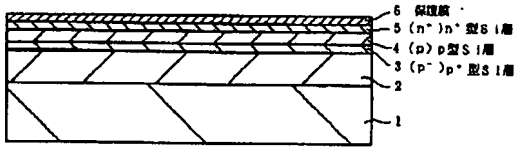
【符号の説明】

１　単結晶Ｓｉ基板
２　多孔質Ｓｉ層
３　p^+型Ｓｉ層
４、４１　ｐ型Ｓｉ層
５　n^+型Ｓｉ層
６、２３　保護膜
７　酸化膜
９、１１、１５、１９、２１　接着剤
１０、１２　治具
１４　ガラス基板
１６　受光面電極
１８、２２　プラスチック基板

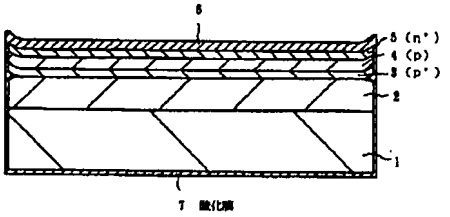
【図１】



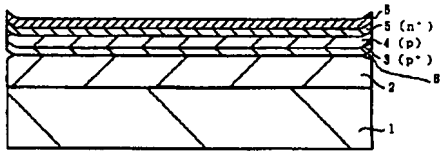
【図２】



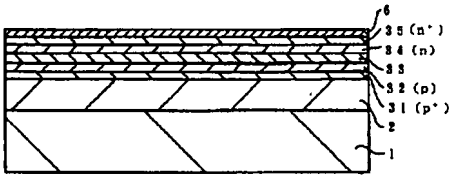
【図３】



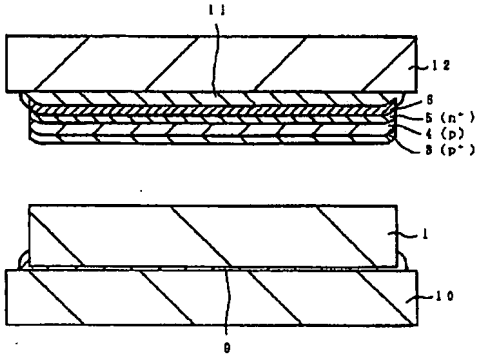
【図４】



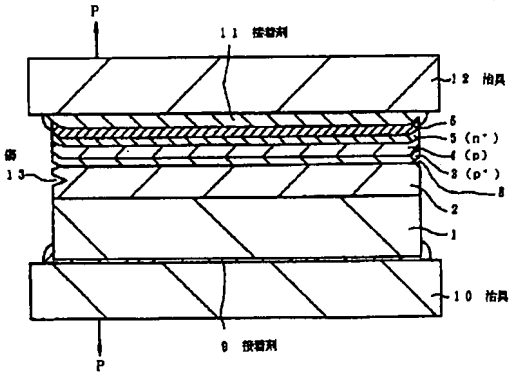
【図１３】



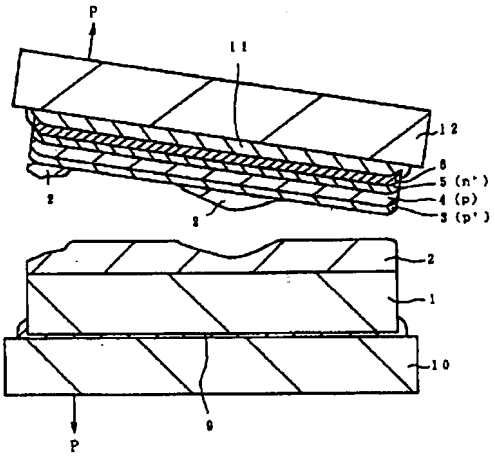
【図７】



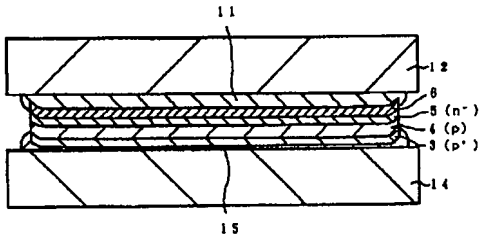
【図５】



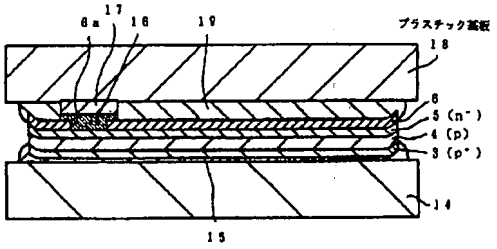
【図６】



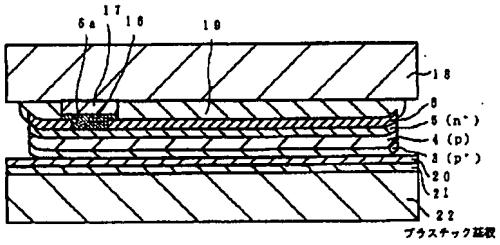
【図８】



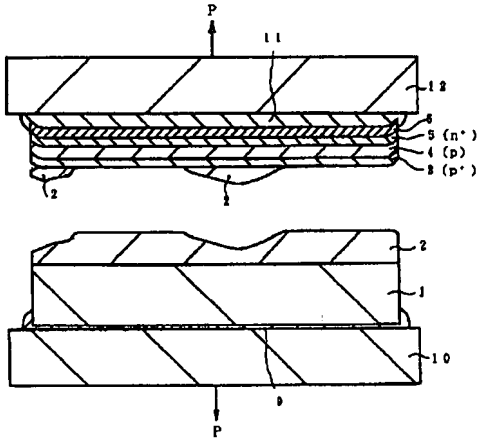
【図９】



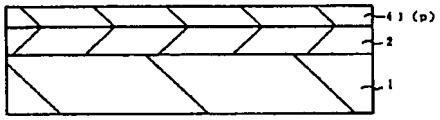
【図１０】



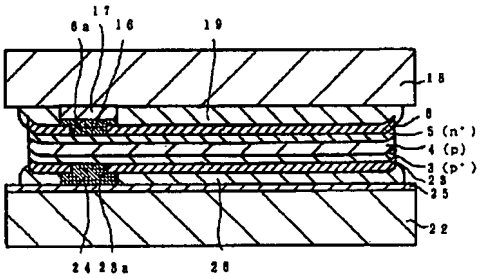
【図１１】



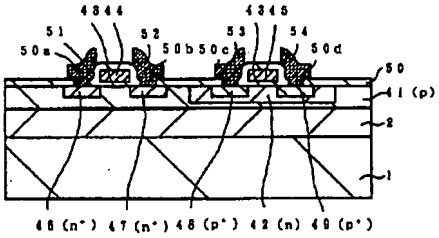
【図１４】



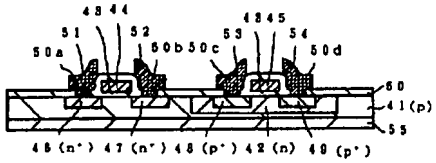
【図１２】



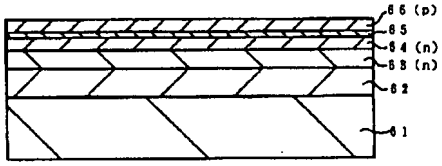
【図１５】



【図１６】



【図１７】



フロントページの続き

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			31/04	Ｅ	